



```
module eight_to_three_encoder_tbsim;
reg [7:0] x;
wire [2:0] y;
integer i;
initial begin
    x = 8'b00000000; #10;
    for (i=0;i<10;i=i+1)
        begin
            if (i<5)
                {x} = {x} + 8'b00000001;
            else
                x = x << 1;
            #10;
        end
    end
    eight_to_three_encoder UUT(.x(x),.y(y));
endmodule
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```
module eight_to_three_encoder(x,y);
input [7:0] x;
output [2:0] y;
assign y[0]=(~x[7]&~x[6]&~x[5]&~x[4]&~x[3]&~x[2]&x[1])+(~x[7]&~x[6]&~x[5]&~x[4]&x[3])+(~x[7]&~x[6]&x[5])+x[7];
assign y[1]=((~x[5]&~x[4])&(x[3]+x[2]))+x[6]+x[7];
assign y[2]=((~x[7]&~x[6])&(x[5]+x[4]))+x[6]+x[7];
endmodule
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```

