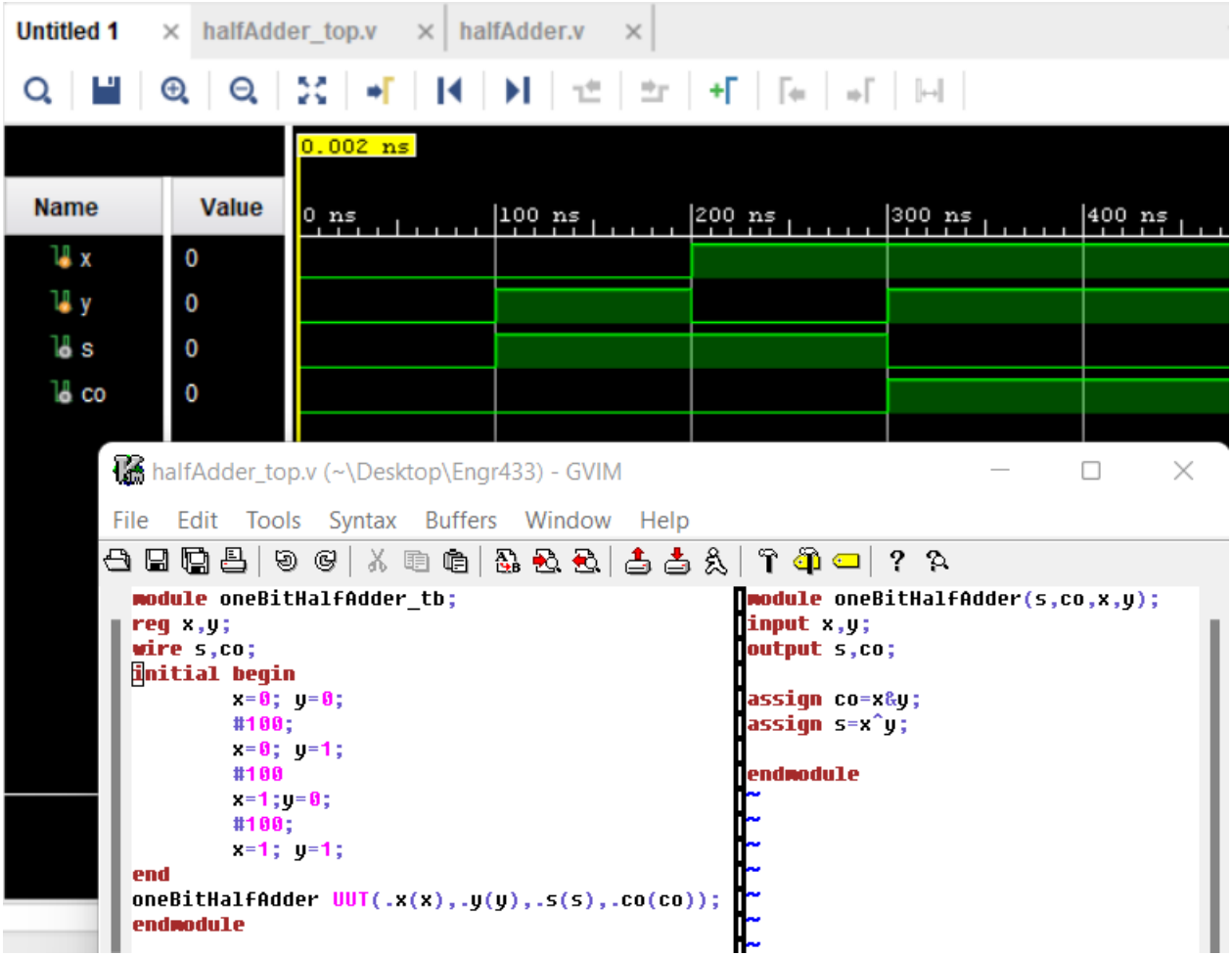
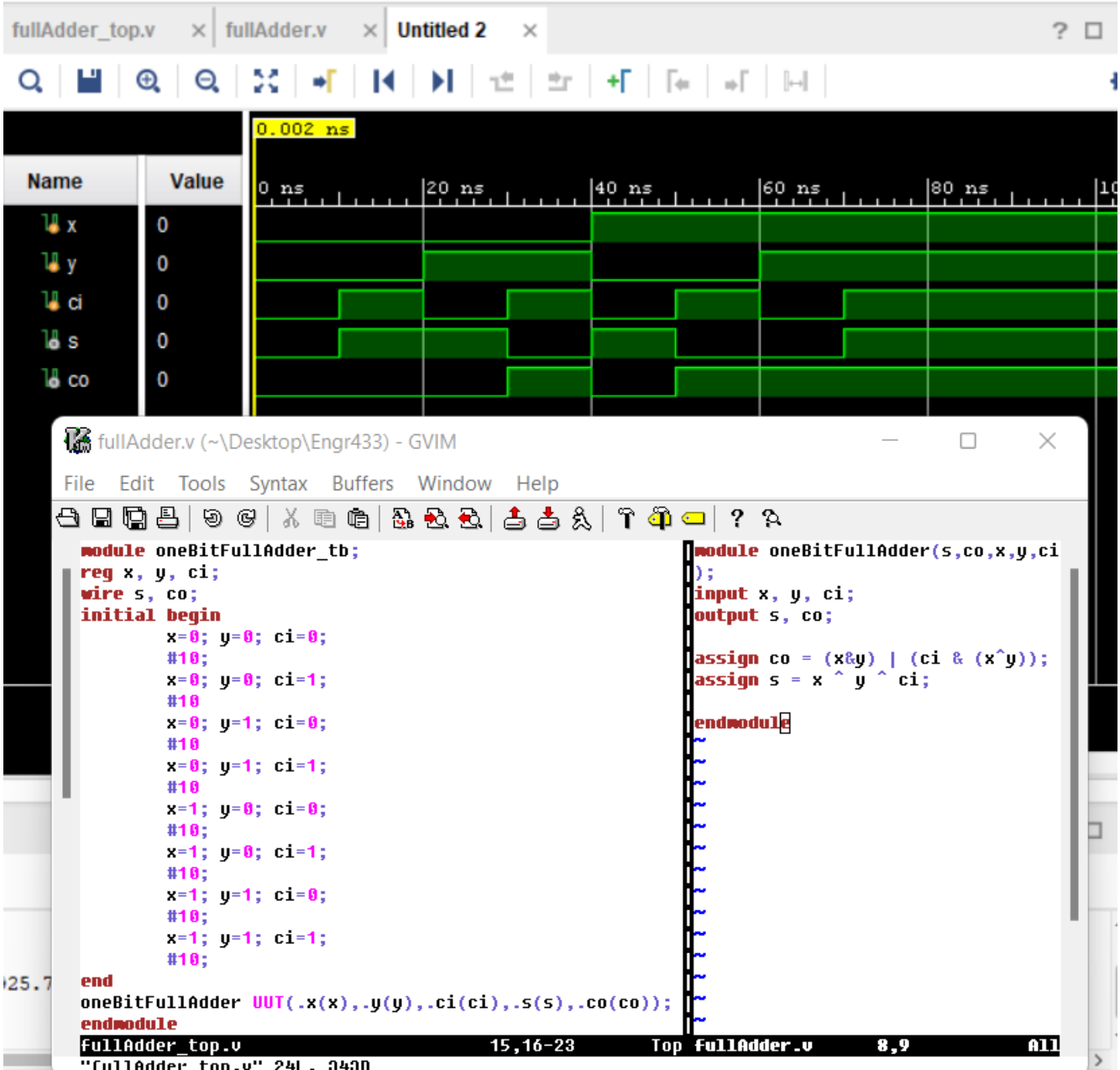
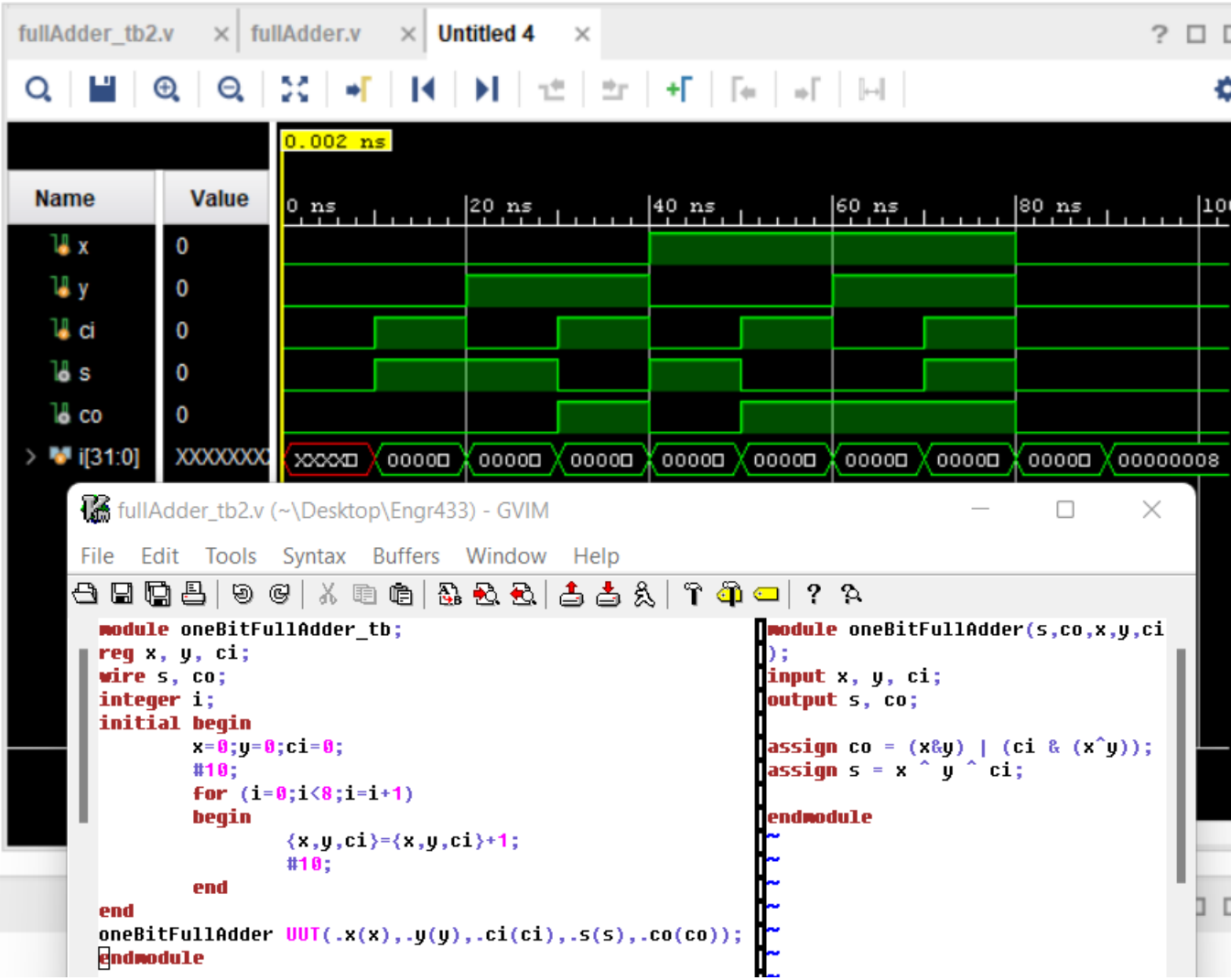

Untitled 1
halfAdder_top.v
halfAdder.v
0.002 ns
Name
Value
0 ns
100 ns
200 ns
300 ns
400 ns
x
0
y
0
s
0
co
0
halfAdder_top.v (~\Desktop\Engr433) - GVIM
File Edit Tools Syntax Buffers Window Help
module oneBitHalfAdder_tb;
reg x,y;
wire s,co;
initial begin
x=0; y=0;
#100;
x=0; y=1;
#100
x=1;y=0;
#100;
x=1; y=1;
end
oneBitHalfAdder UUT(.x(x),.y(y),.s(s),.co(co));
endmodule
module oneBitHalfAdder(s,co,x,y);
input x,y;
output s,co;
assign co=x&y;
assign s=x^y;
endmodule


fullAdder_top.v
fullAdder.v
Untitled 2
0.002 ns
Name
Value
0 ns
20 ns
40 ns
60 ns
80 ns
x
y
ci
s
co
0
fullAdder.v (~\Desktop\Engr433) - GVIM
File Edit Tools Syntax Buffers Window Help
module oneBitFullAdder_tb;
reg x, y, ci;
wire s, co;
initial begin
x=0; y=0; ci=0;
#10;
x=0; y=0; ci=1;
#10
x=0; y=1; ci=0;
#10
x=0; y=1; ci=1;
#10
x=1; y=0; ci=0;
#10;
x=1; y=0; ci=1;
#10;
x=1; y=1; ci=0;
#10;
x=1; y=1; ci=1;
#10;
end
oneBitFullAdder UUT(.x(x),.y(y),.ci(ci),.s(s),.co(co));
endmodule
module oneBitFullAdder(s,co,x,y,ci
);
input x, y, ci;
output s, co;
assign co = (x&y) | (ci & (x^y));
assign s = x ^ y ^ ci;
endmodule
FullAdder_top.v 15,16-23 Top fullAdder.v 8,9 All


fullAdder_tb2.v
fullAdder.v
Untitled 4
0.002 ns
Name
Value
0 ns
20 ns
40 ns
60 ns
80 ns
x
y
ci
s
co
i[31:0]
00000008
fullAdder_tb2.v (~\Desktop\Engr433) - GVIM
File Edit Tools Syntax Buffers Window Help
module oneBitFullAdder_tb;
reg x, y, ci;
wire s, co;
integer i;
initial begin
x=0;y=0;ci=0;
#10;
for (i=0;i<8;i=i+1)
begin
{x,y,ci}={x,y,ci}+1;
#10;
end
end
oneBitFullAdder UUT(.x(x),.y(y),.ci(ci),.s(s),.co(co));
endmodule
module oneBitFullAdder(s,co,x,y,ci
);
input x, y, ci;
output s, co;
assign co = (x&y) | (ci & (x^y));
assign s = x ^ y ^ ci;
endmodule