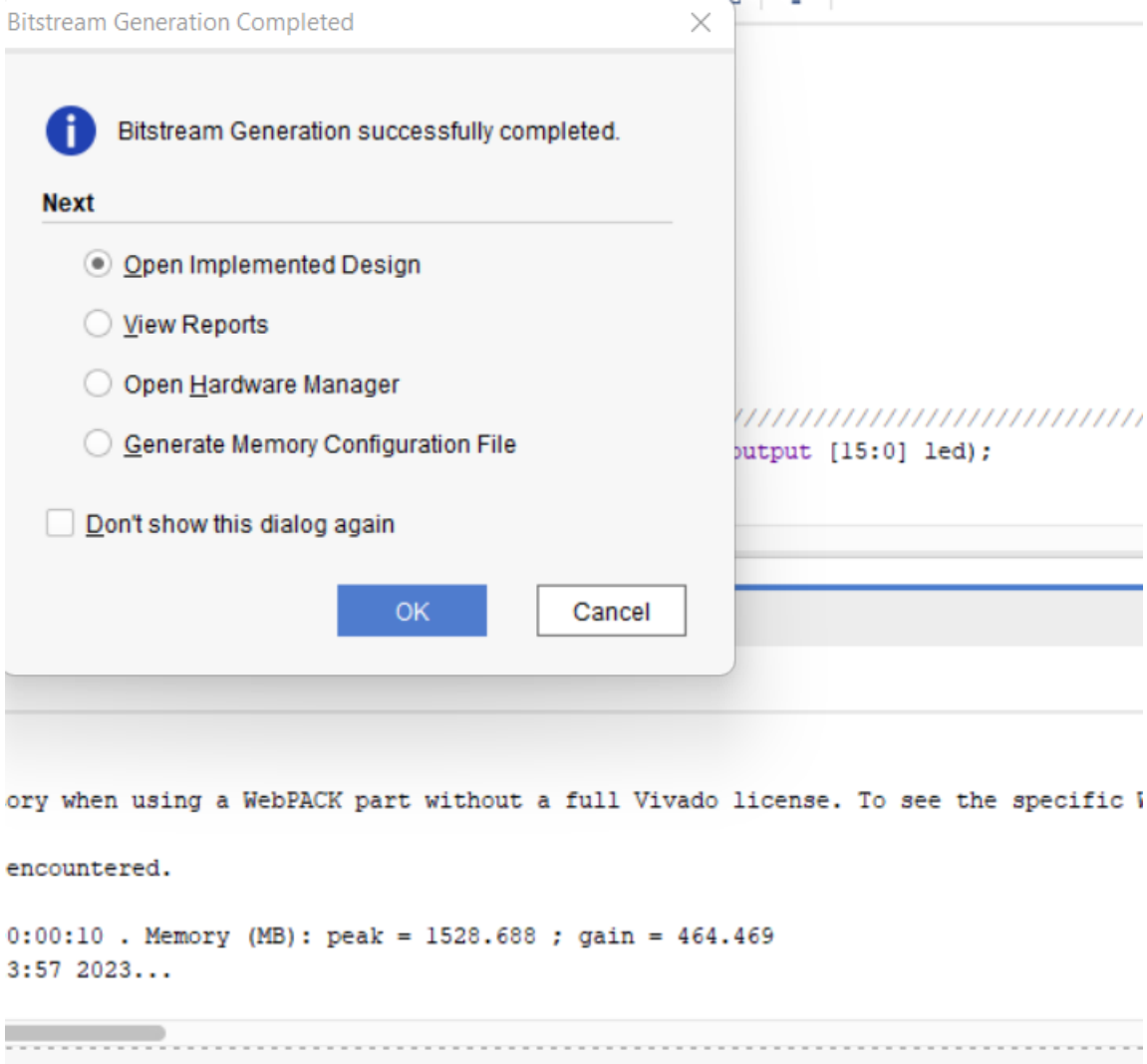
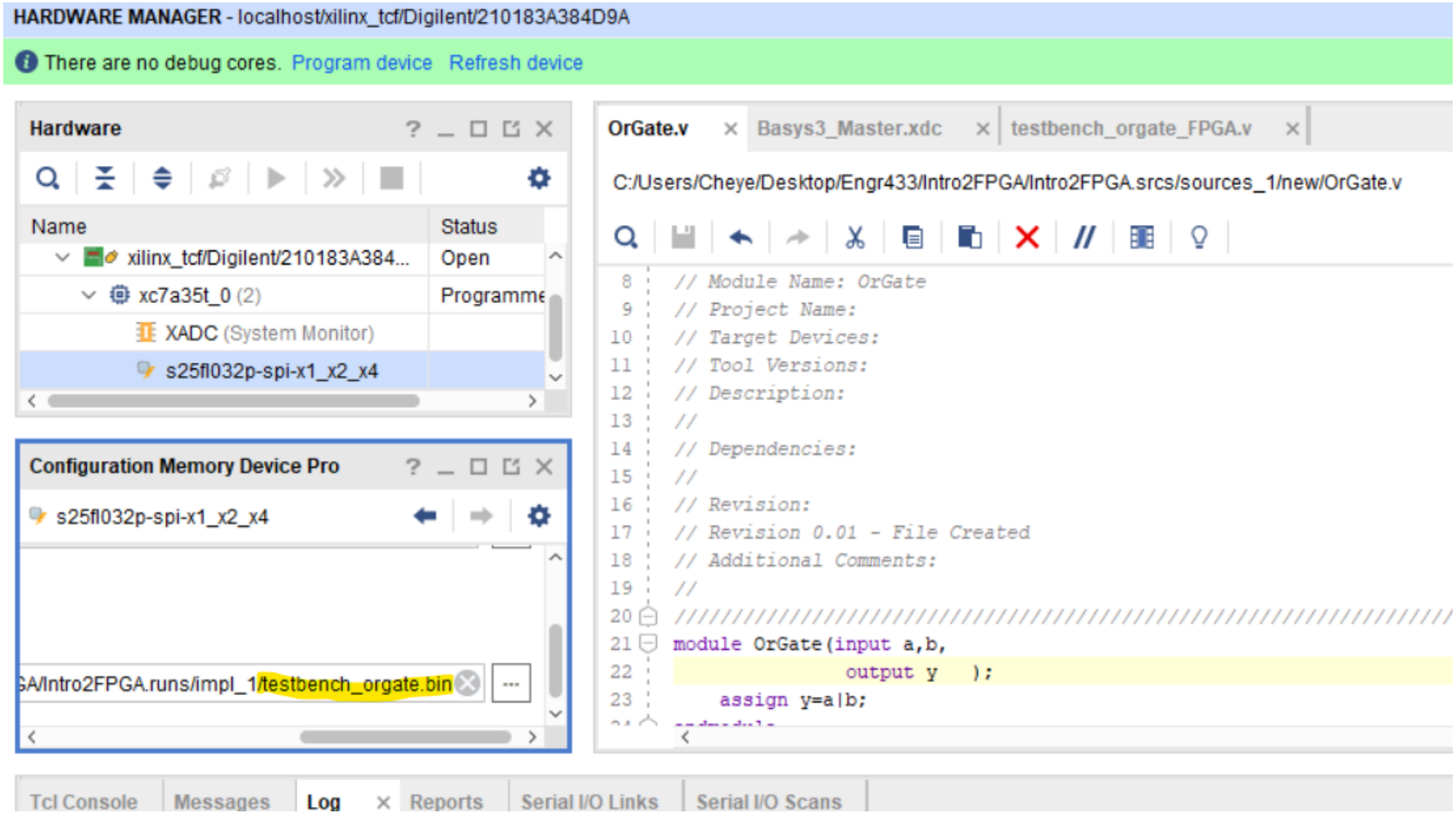
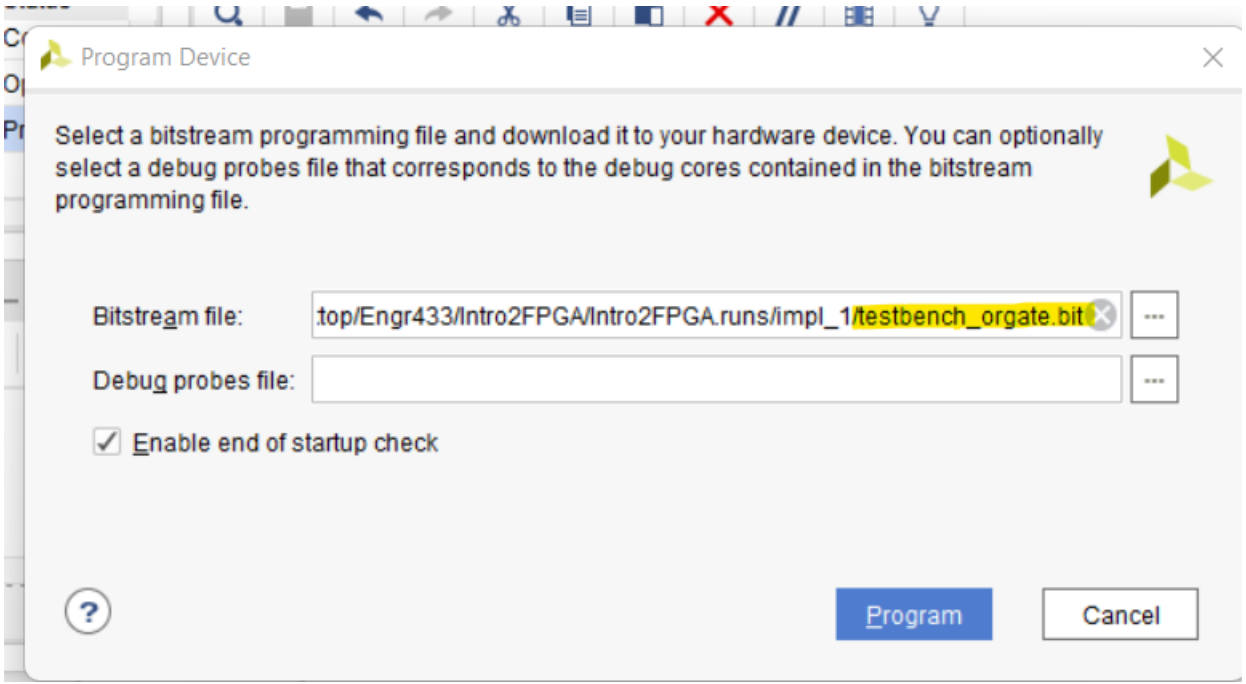

Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel
utput [15:0] led);
ory when using a WebPACK part without a full Vivado license. To see the specific
encountered.
0:00:10 . Memory (MB): peak = 1528.688 ; gain = 464.469
3:57 2023...


HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210183A384D9A
There are no debug cores. Program device Refresh device
Hardware
Name
Status
xilinx_tcf/Digilent/210183A384...
Open
xc7a35t_0 (2)
Programme
XADC (System Monitor)
s25fl032p-spi-x1_x2_x4
Configuration Memory Device Pro
s25fl032p-spi-x1_x2_x4
GA/Intro2FPGA.runs/impl_1/testbench_orgate.bin
OrGate.v
Basys3_Master.xdc
testbench_orgate_FPGA.v
C:/Users/Cheye/Desktop/Engr433/Intro2FPGA/Intro2FPGA.srcs/sources_1/new/OrGate.v
8 // Module Name: OrGate
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module OrGate(input a,b,
22 output y);
23 assign y=a|b;
Tcl Console
Messages
Log
Reports
Serial I/O Links
Serial I/O Scans


Program Device
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.
Bitstream file:
top/Engr433/Intro2FPGA/Intro2FPGA.runs/impl_1/testbench_orgate.bit
Debug probes file:
Enable end of startup check
Program
Cancel