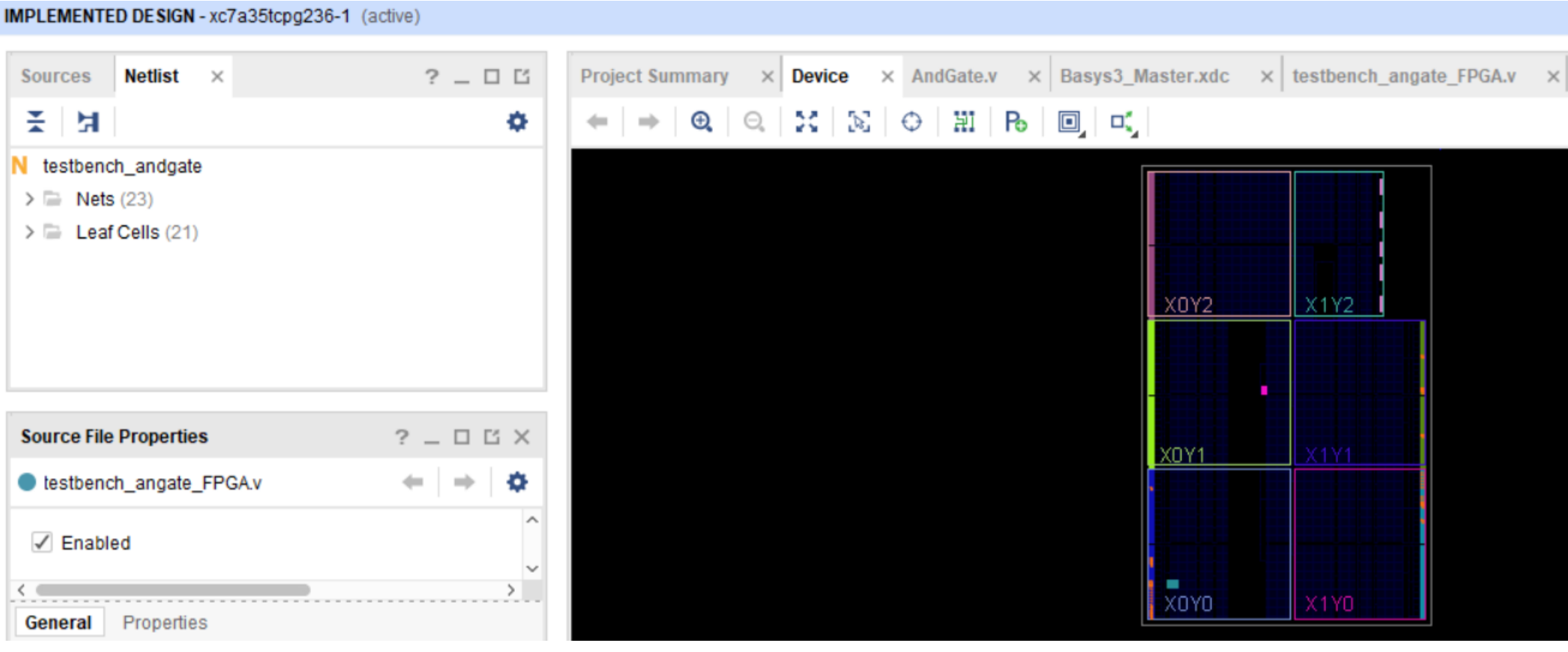
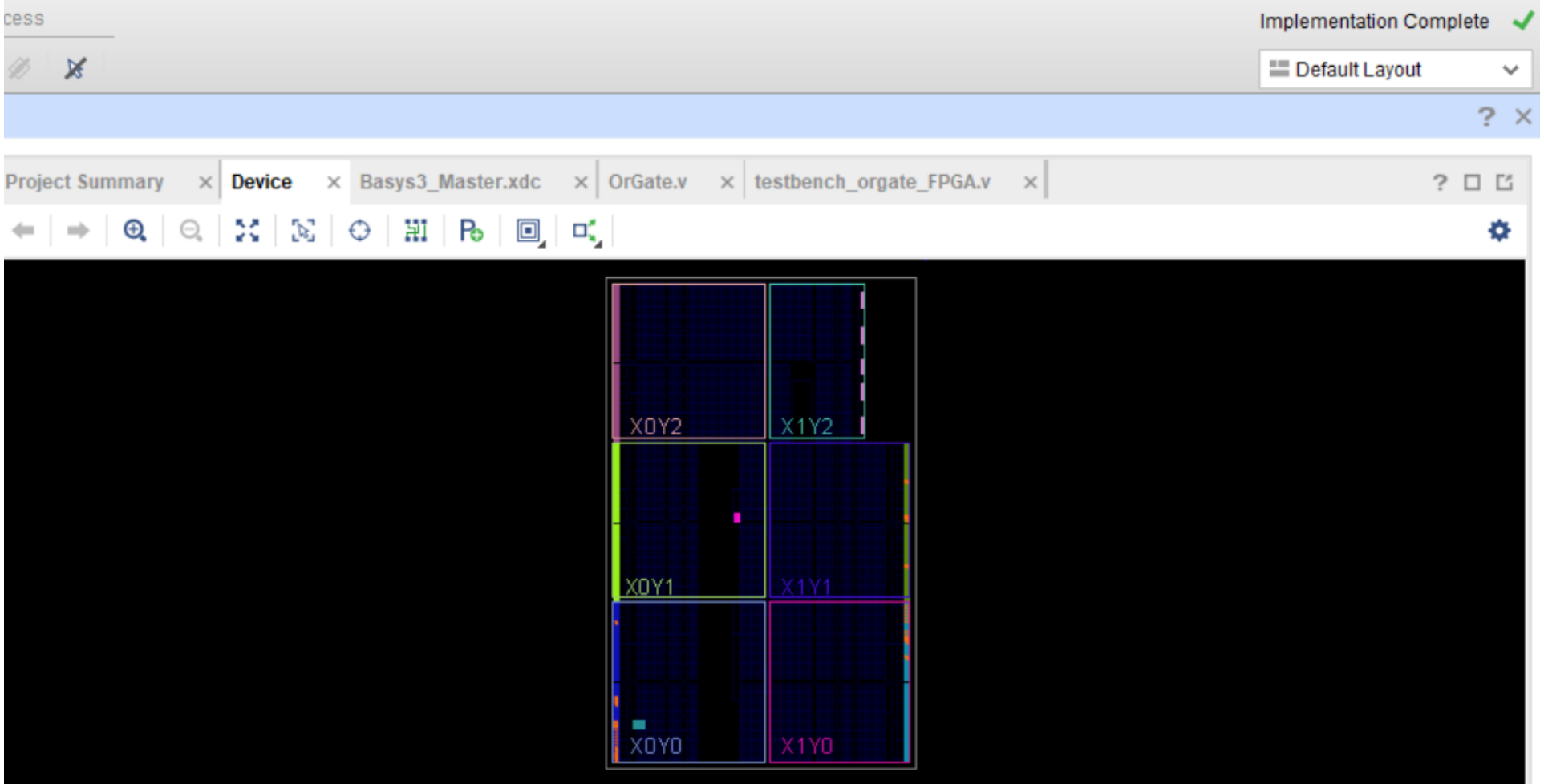
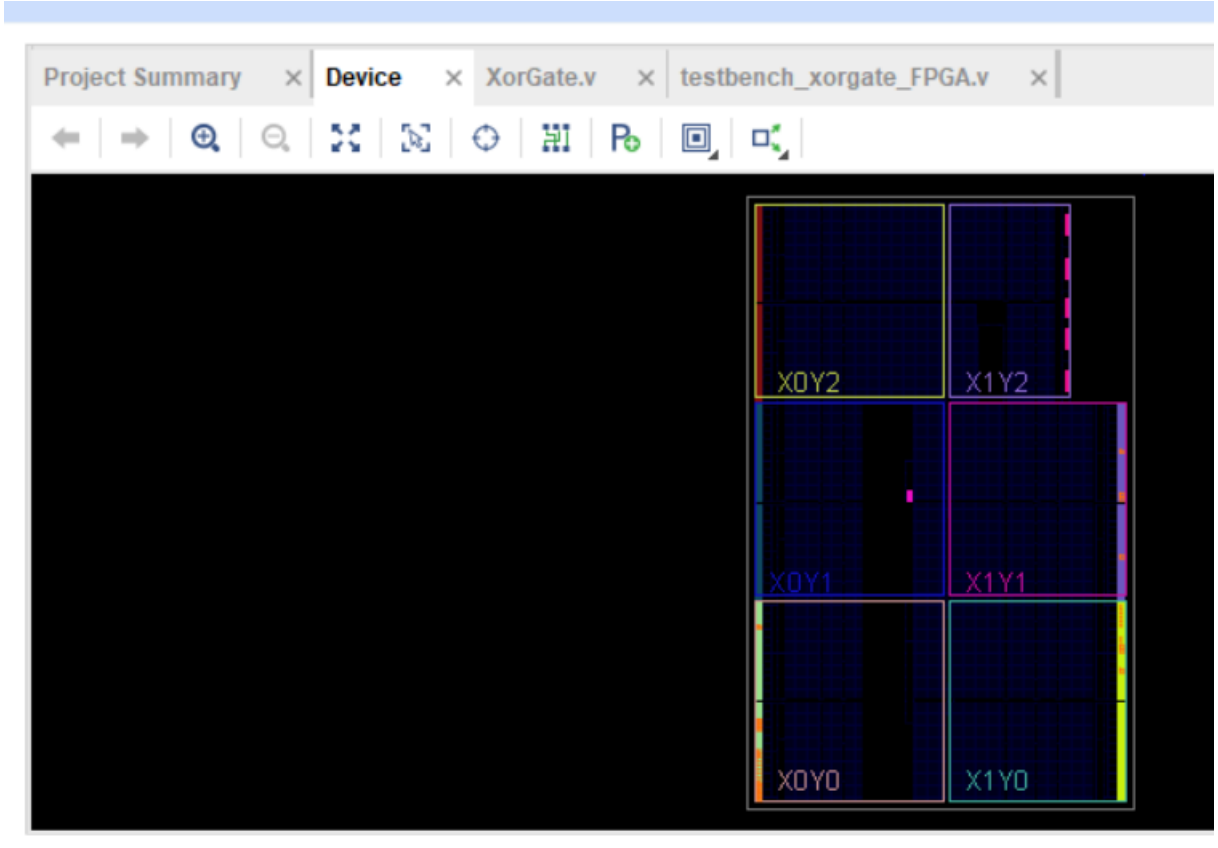

IMPLEMENTED DESIGN - xc7a35tcpg236-1 (active)
Sources
Netlist
testbench_andgate
Nets (23)
Leaf Cells (21)
Source File Properties
testbench_angate_FPGA.v
Enabled
General
Properties
Project Summary
Device
AndGate.v
Basys3_Master.xdc
testbench_angate_FPGA.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


cess
Implementation Complete
Default Layout
Project Summary
Device
Basys3_Master.xdc
OrGate.v
testbench_orgate_FPGA.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


Project Summary
Device
XorGate.v
testbench_xorgate_FPGA.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0