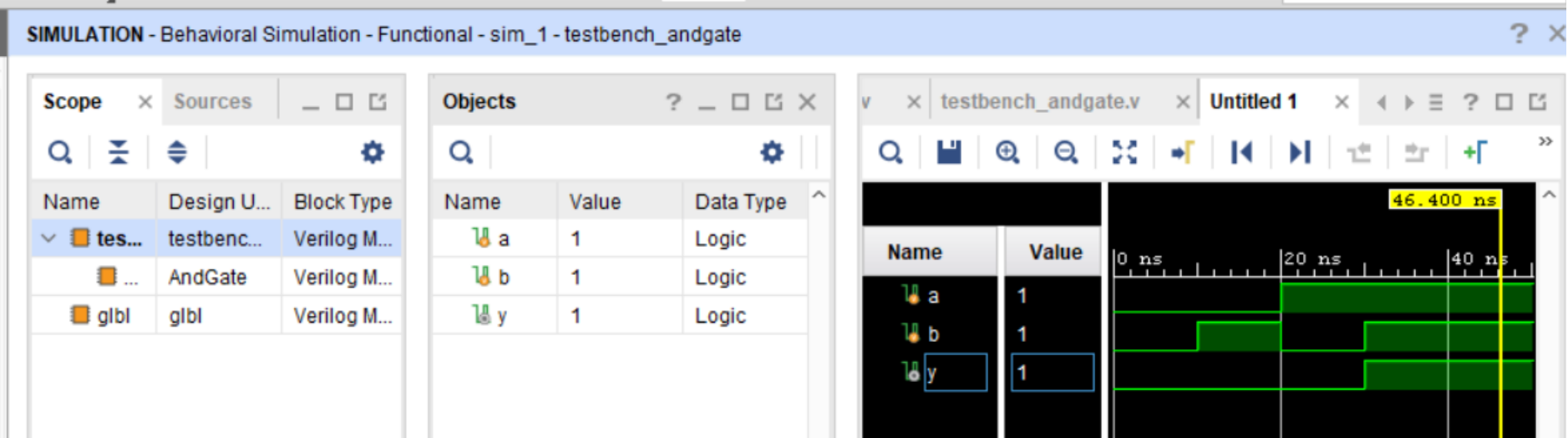
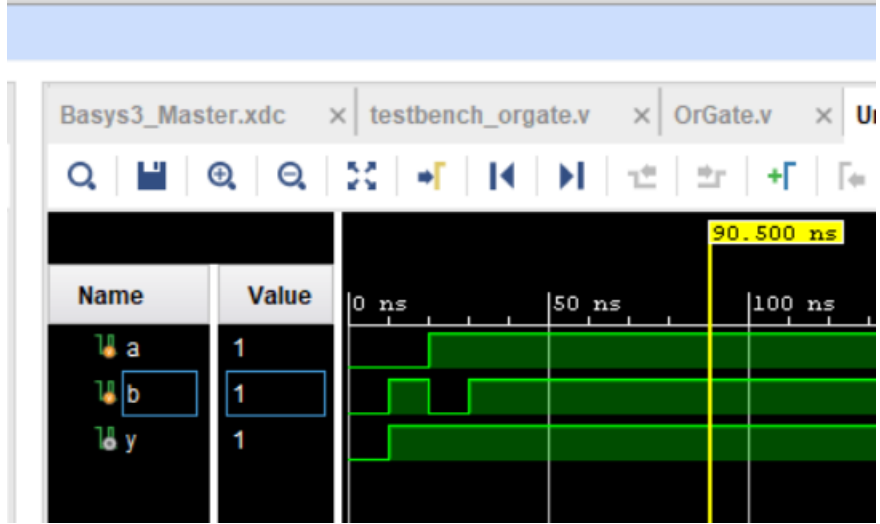
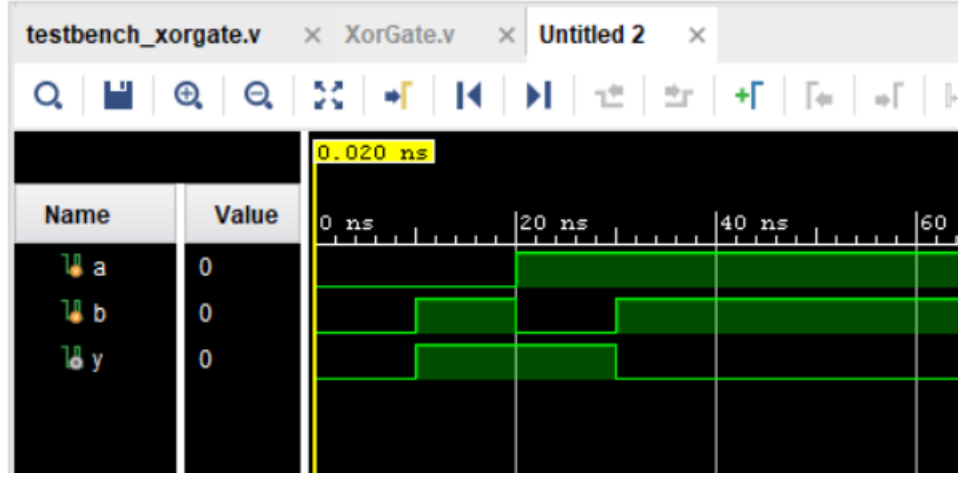

SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench_andgate
Scope
Sources
Name
Design U...
Block Type
tes...
testbenc...
Verilog M...
...
AndGate
Verilog M...
glbl
glbl
Verilog M...
Objects
Name
Value
Data Type
a
1
Logic
b
1
Logic
y
1
Logic
testbench_andgate.v
Untitled 1
Name
Value
a
1
b
1
y
1
46.400 ns
0 ns
20 ns
40 ns


Basys3_Master.xdc
testbench_orgate.v
OrGate.v
Name
Value
a
b
y
1
1
1
90.500 ns
0 ns
50 ns
100 ns


testbench_xorgate.v
XorGate.v
Untitled 2
Name
Value
a
0
b
0
y
0
0.020 ns
0 ns
20 ns
40 ns
60