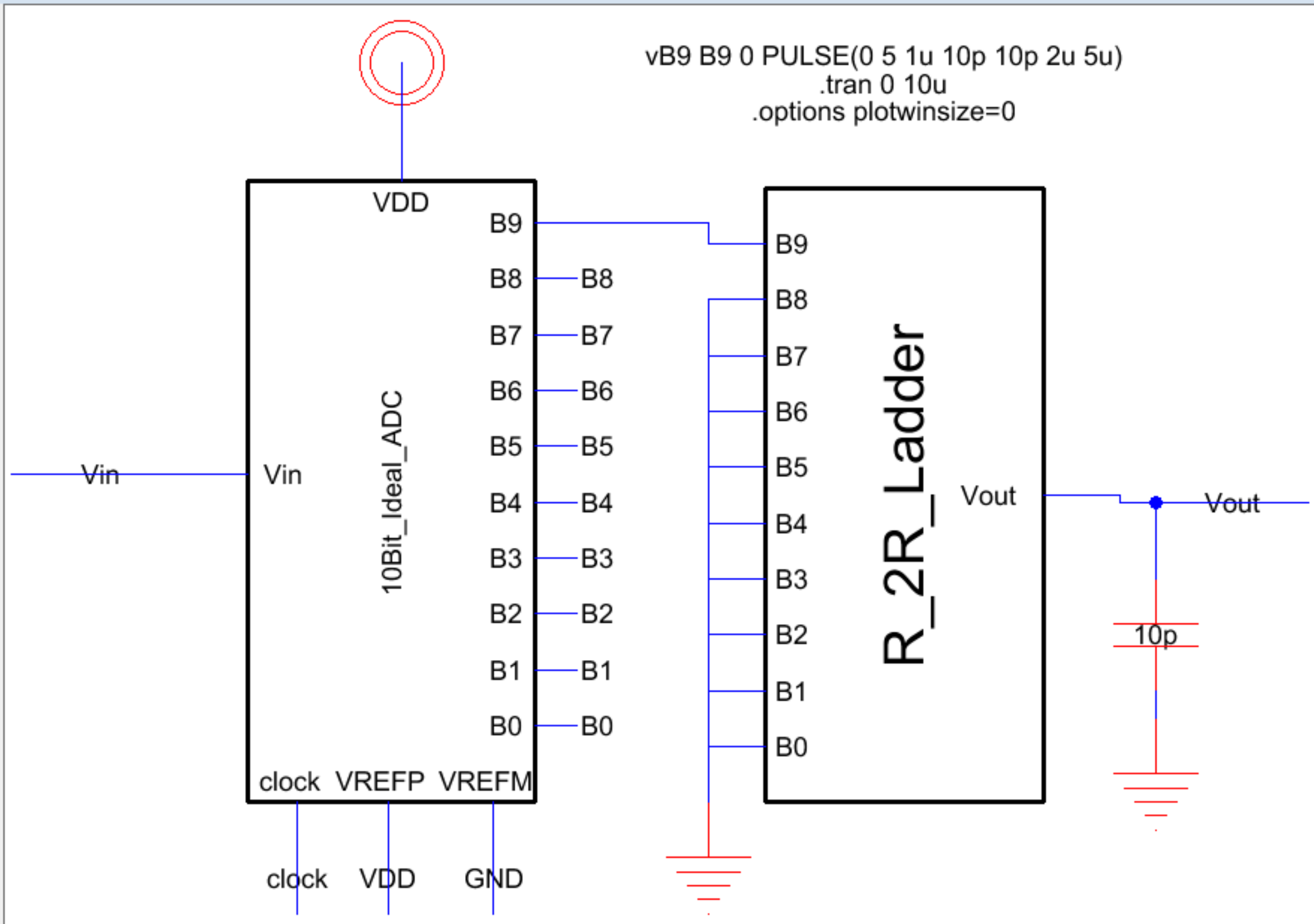
sim_ADC_R_2R_DAC_DelayTest{sch} - Current library: lab2

Explorer | Layers



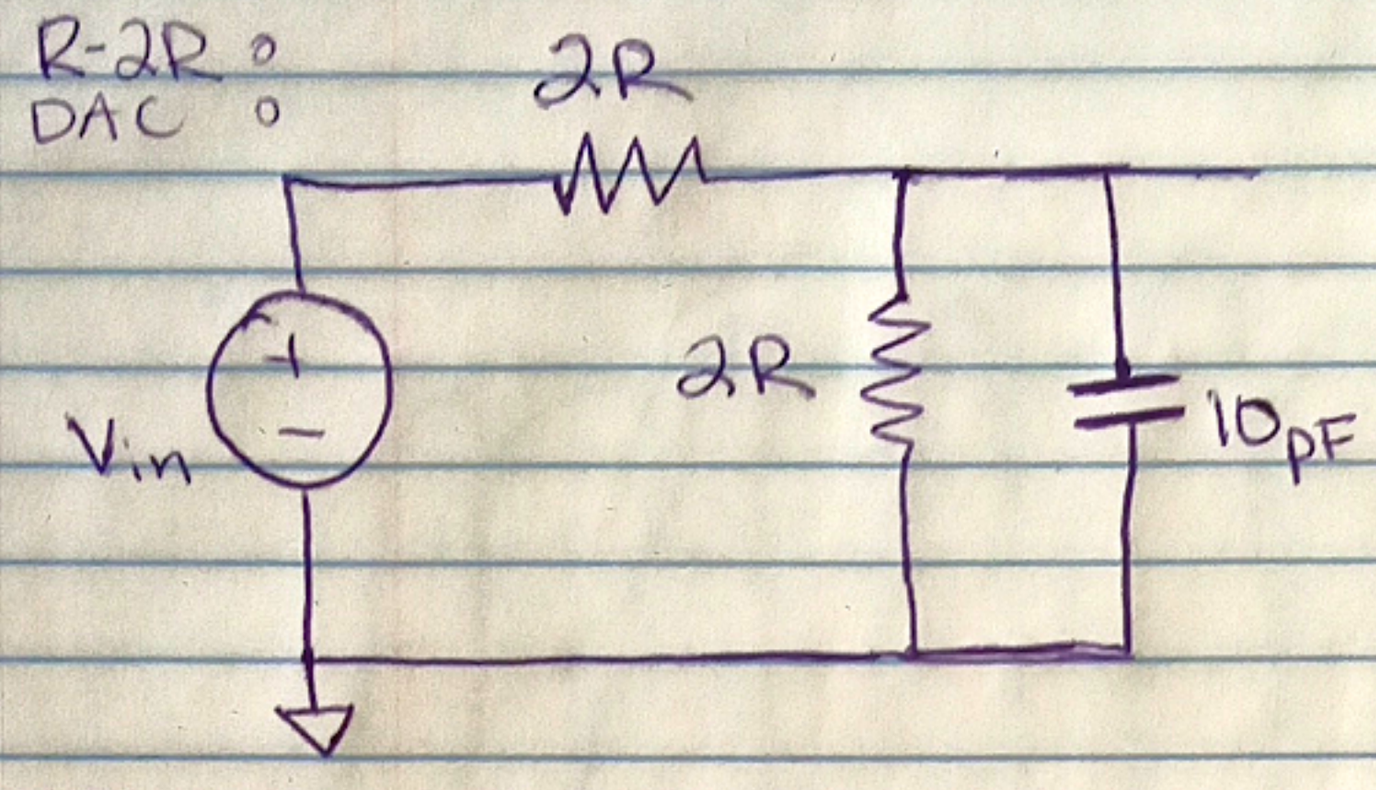
Electric Messages

```
   No errors found
Checking schematic cell 'ENGR338:sim_ADC_R_2R_DAC_DelayTest{sch}'
Network: Schematic ENGR338:sim_ADC_R_2R_DAC_DelayTest{sch} doesn't connect network 'GND' and network 'gnd'
Network: Schematic ENGR338:sim_ADC_R_2R_DAC_DelayTest{sch} doesn't connect network 'VDD' and network 'vdd'
   No errors found
0 errors and 2 warnings found (took 0.015 secs)
Schematic DRC (full) found 0 errors, 2 warnings!
Type > and < to step through warnings, or open the ERRORS view in the explorer
```

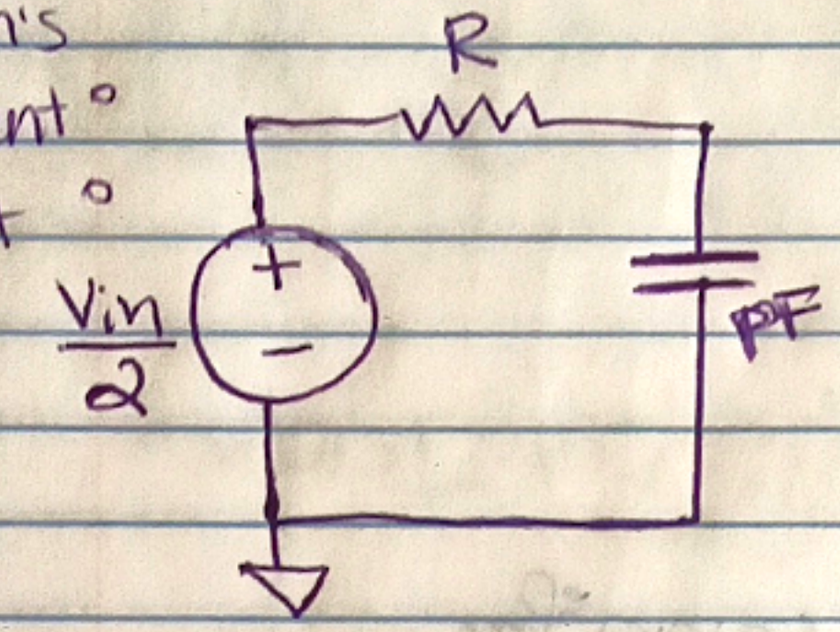
Lab 2 - Task 3

Time Delay of the circuit

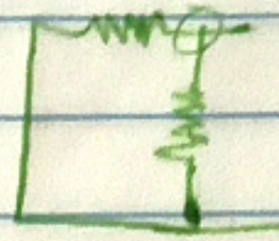
R-2R DAC



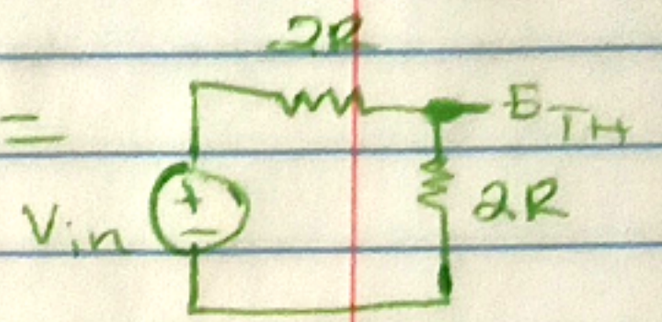
Thevenin's Equivalent Circuit



here R = 10k

$R_{TH} =$  $2R \,||\, 2R$

$= \frac{4R}{4R} = R$

$E_{TH} =$ 

$V_{in}\left(\frac{2R}{4R}\right) = V_{in}\left(\frac{1}{2}\right)$

$= \frac{V_{in}}{2}$

Time Delay:

$t_d = R_{TH}(C_{Load})(0.7RC)$

$= R(10pF)(0.7RC)$

$= (10k\Omega)(10pF)(0.7RC)$

$= 70\,nsec$