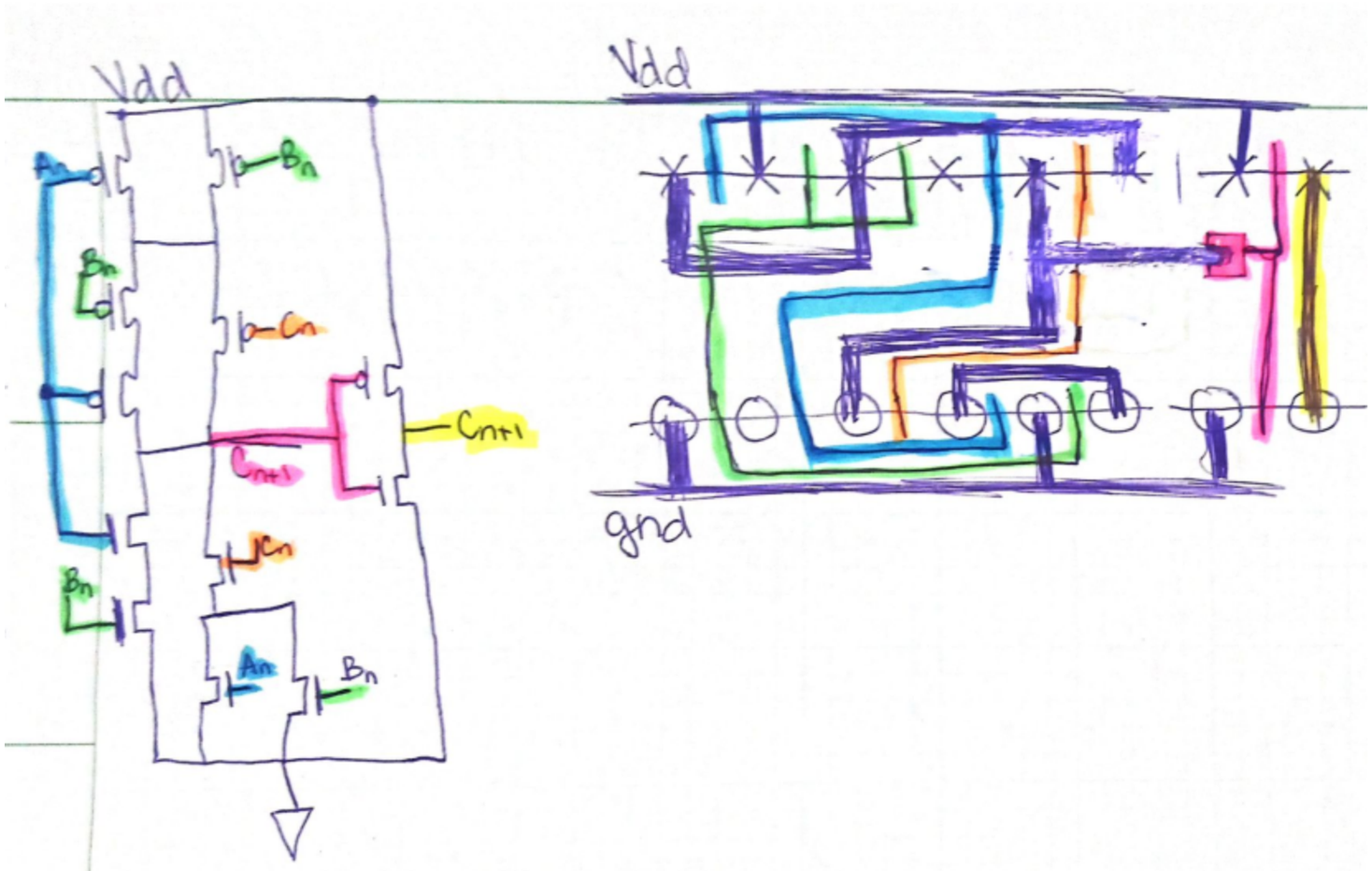
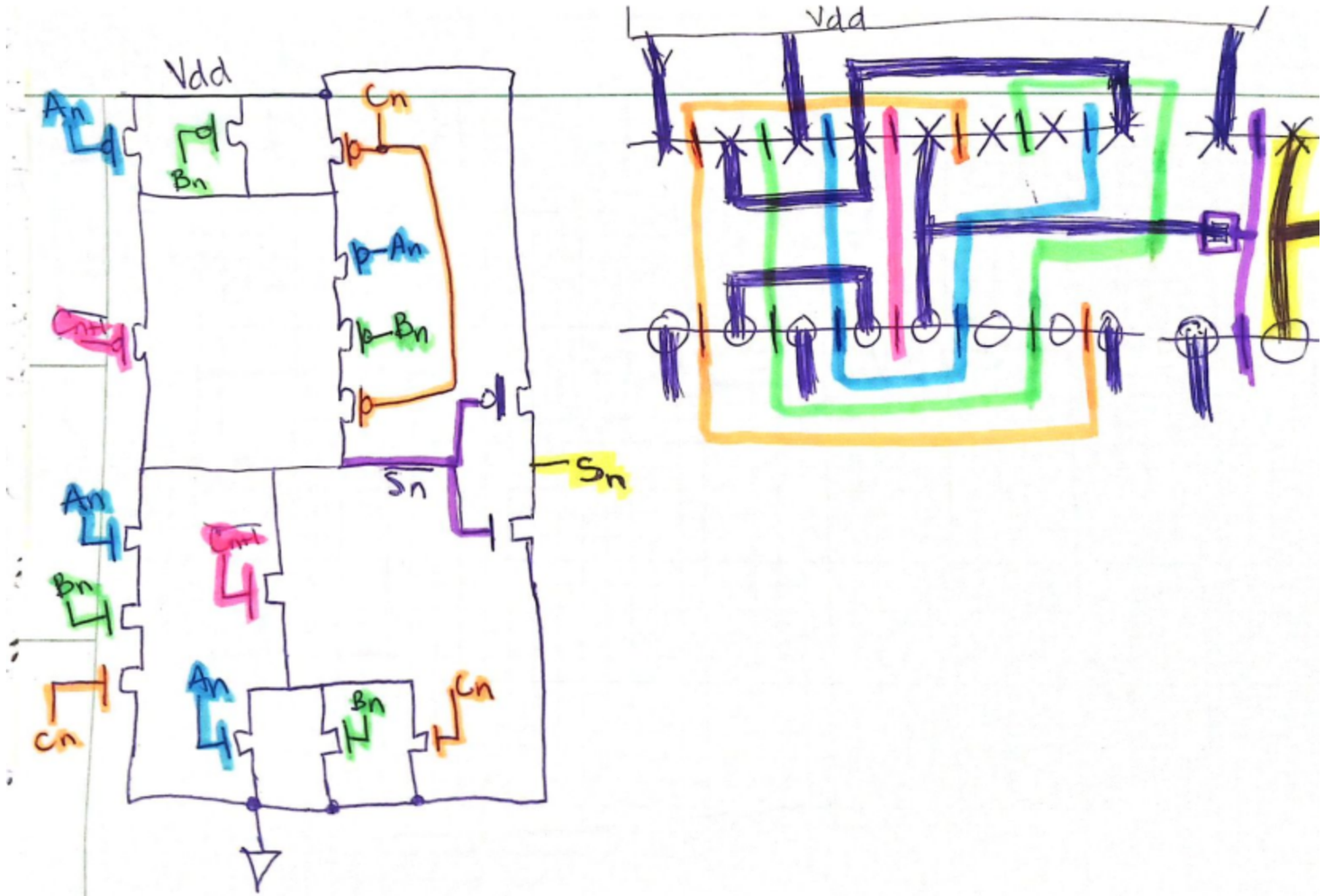
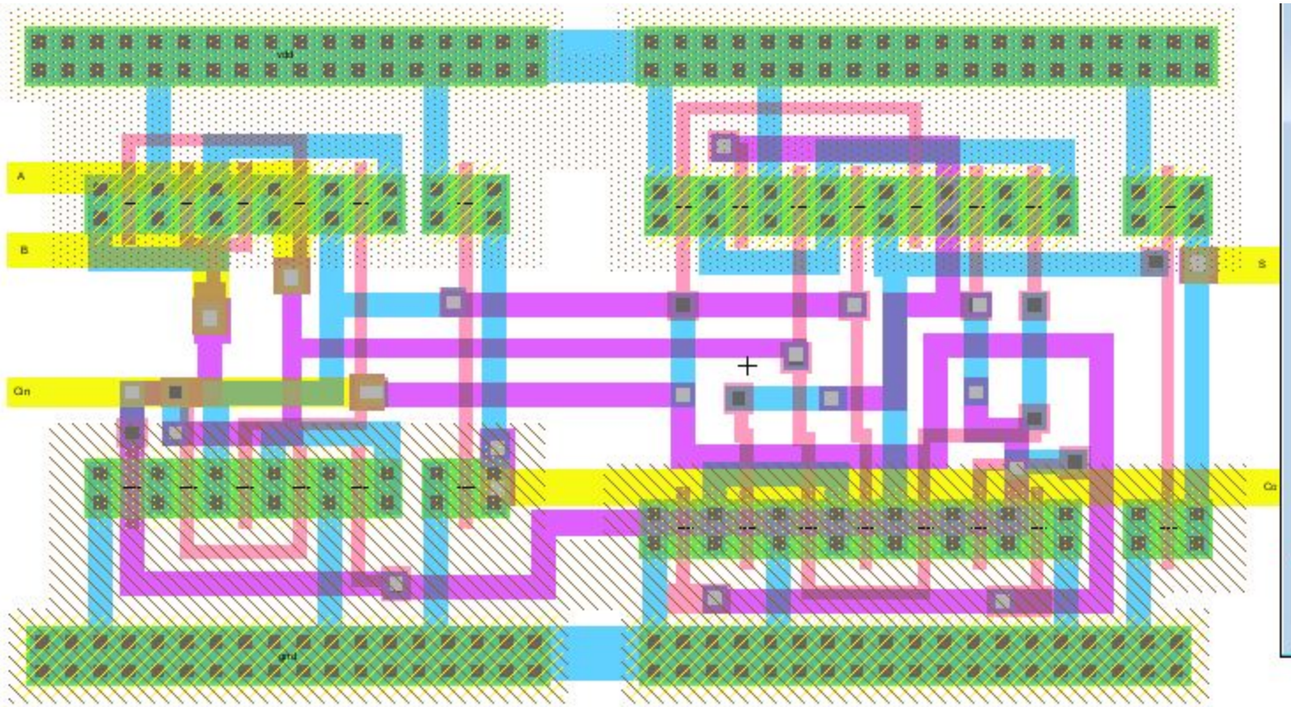

Vdd
An
Bn
Bn
Cn
Cn+1
Cn+1
Cn
Bn
An
Bn
Vdd
gnd


Vdd
An
Bn
Cn
p
p
p
An
Bn
Cn+1
Sn
Sn
An
Bn
Cn+1
Cn
An
Bn
Cn
Vdd

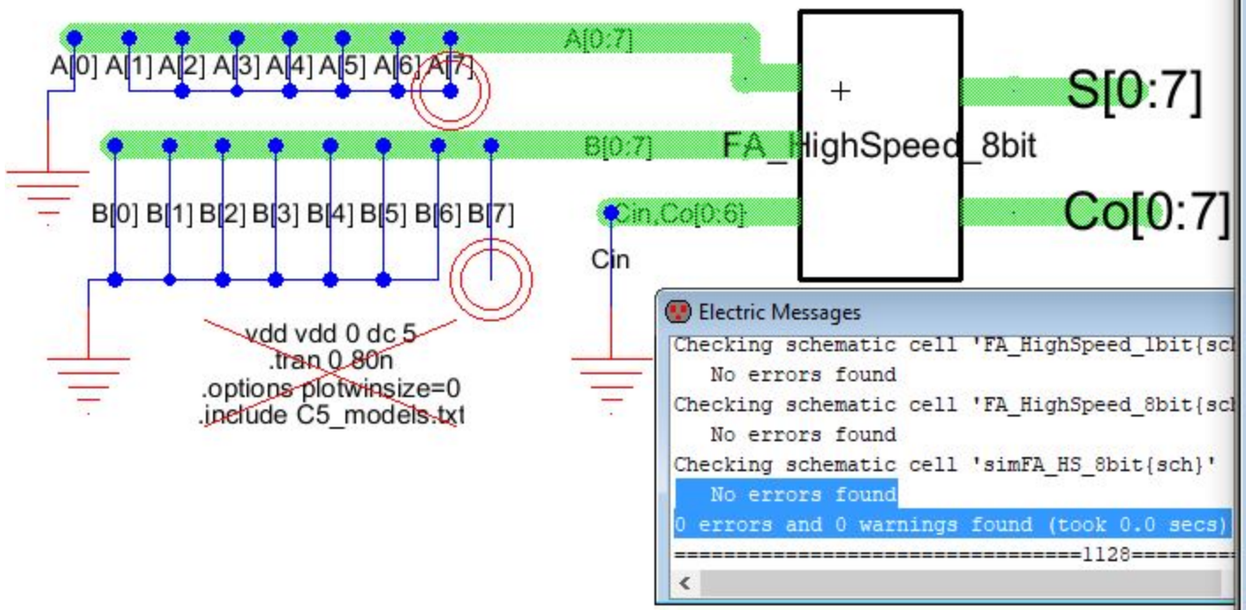



```
==================================944==================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 99 networks
0 errors and 0 warnings found (took 0.0 secs)
==================================945==================================
Checking Wells and Substrates in 'ENGR338_Tucson:FA_HighSpeed_1bit{lay}' ...
   Geometry collection found 170 well pieces, took 0.0 secs
   Geometry analysis used 6 threads and took 0.0 secs
NetValues propagation took 0.0 secs
Checking short circuits in 4 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.0 secs)
==================================946==================================
Hierarchical NCC every cell in the design: cell 'FA_HighSpeed_1bit{sch}'  cell 'FA_HighSpeed_1bit{lay}'
Comparing: ENGR338_Tucson:FA_HighSpeed_1bit{sch} with: ENGR338_Tucson:FA_HighSpeed_1bit{lay}
  exports match, topologies match, sizes not checked in 0.015 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.015 seconds.
```

(254)
A = 11111110

(128)
B = 10000000

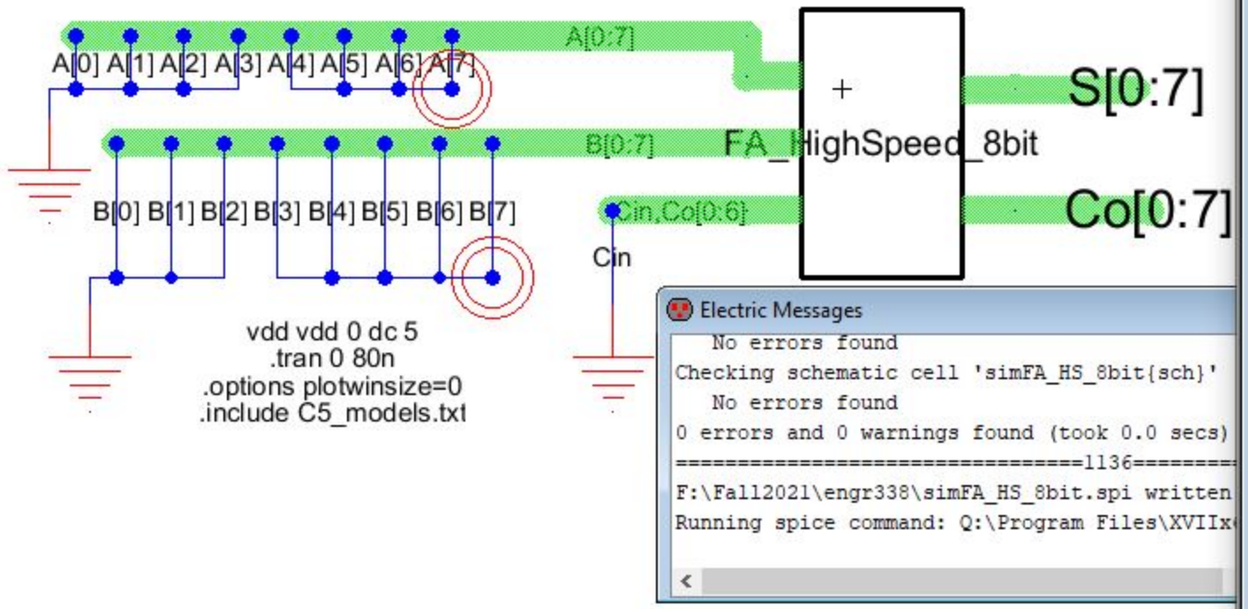
(382)
A+B = 01111110 $C_0 = 1$



(240)
A=11110000

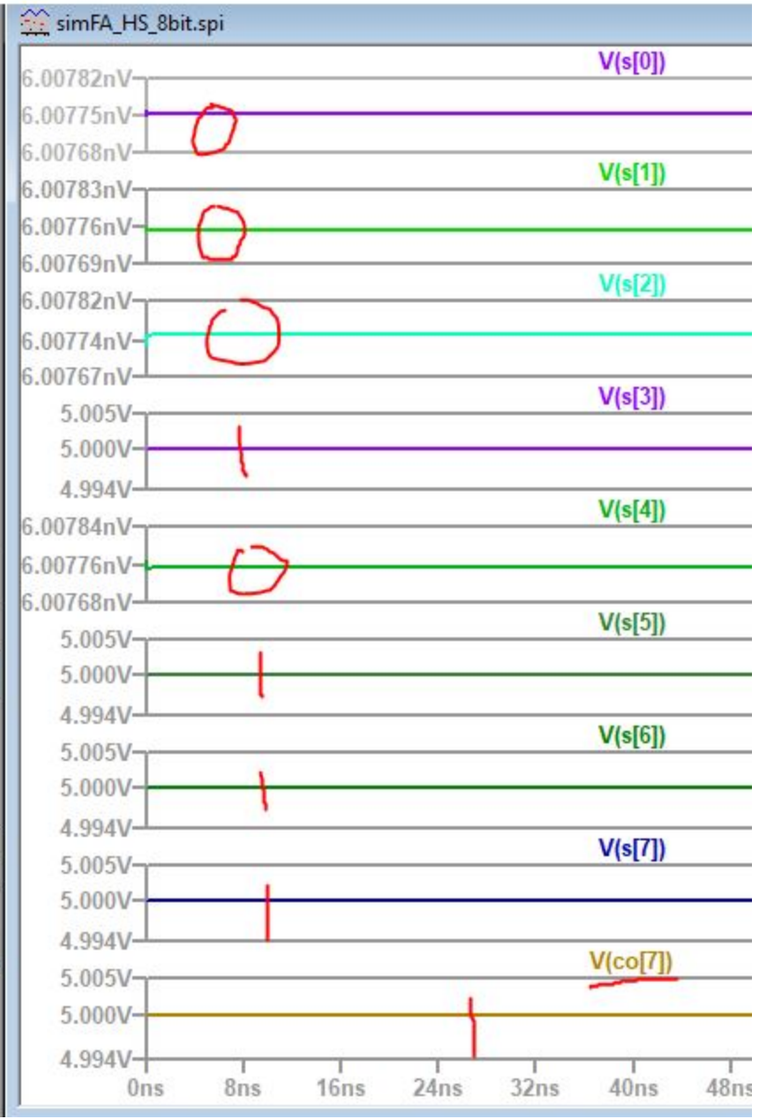
(248)
B=11111000

(488)
A+B=11101000 co=1



Electric Messages

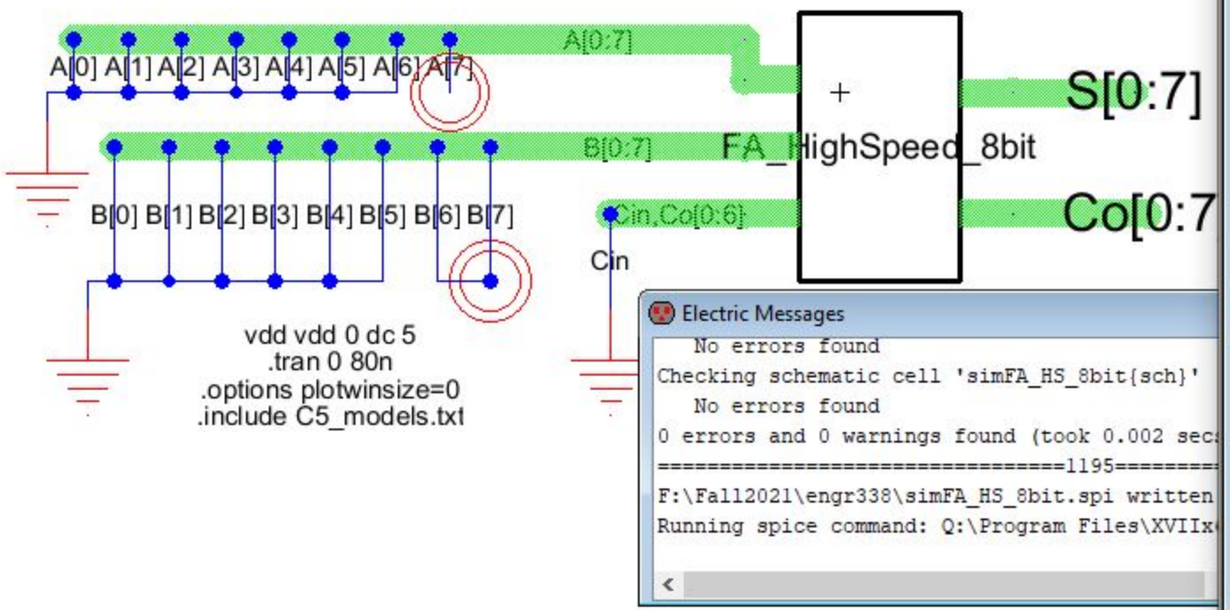
```
   No errors found
Checking schematic cell 'simFA_HS_8bit{sch}'
   No errors found
0 errors and 0 warnings found (took 0.0 secs)
================================1136========
F:\Fall2021\engr338\simFA_HS_8bit.spi written
Running spice command: Q:\Program Files\XVIIx
```

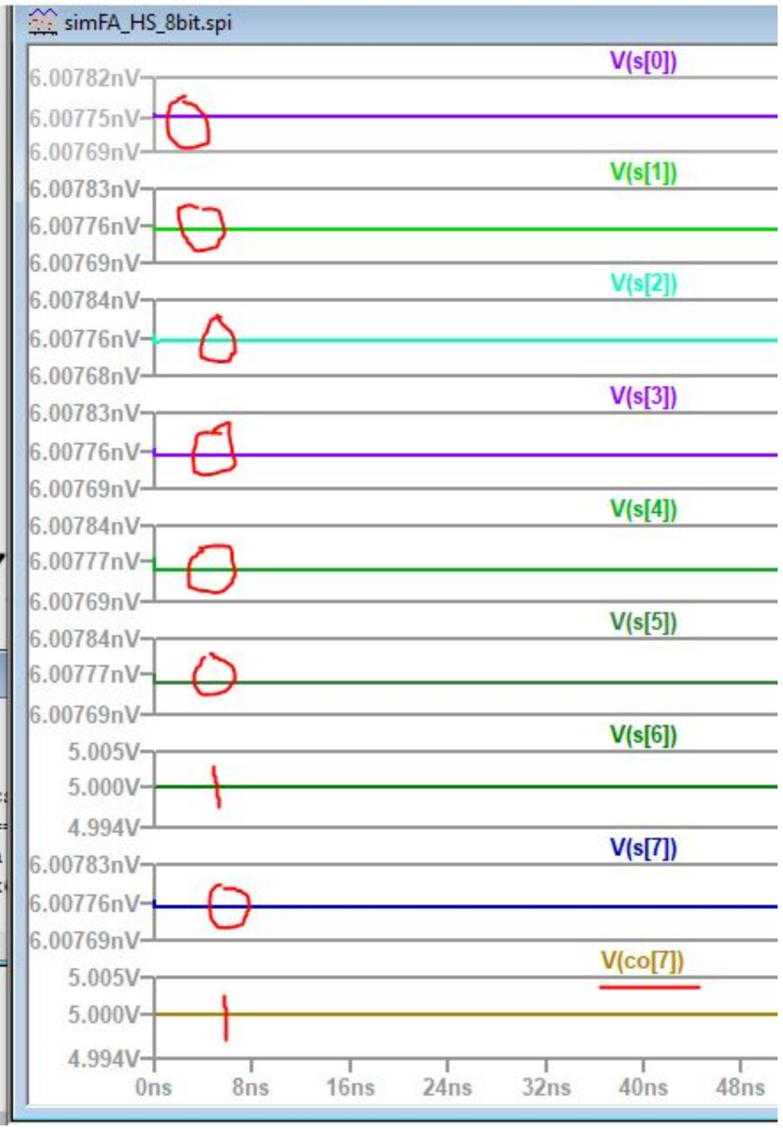


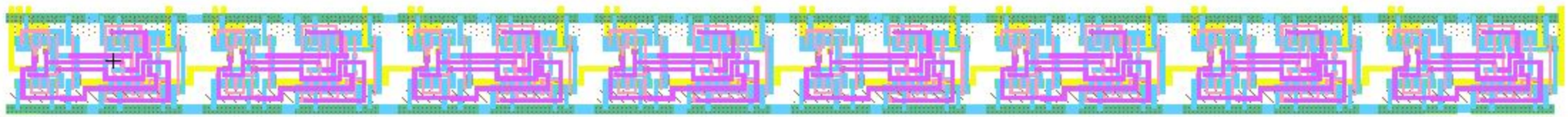
(128)
A = 10000000

(192)
B = 11000000

(320)
A+B = 101000000 Co=1







Electric Messages

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 36 networks
0 errors and 0 warnings found (took 0.0 secs)
================================1811================================
Checking Wells and Substrates in 'ENGR338_Tucson:FA_HighSpeed_8bit{lay}' ...
   Geometry collection found 1360 well pieces, took 0.0 secs
   Geometry analysis used 6 threads and took 0.0 secs
NetValues propagation took 0.0 secs
Checking short circuits in 32 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.0 secs)
================================1812================================
Hierarchical NCC every cell in the design: cell 'FA_HighSpeed_8bit{sch}'  cell 'FA_HighSpeed_8bit{lay}'
Comparing: ENGR338_Tucson:FA_HighSpeed_1bit{sch} with: ENGR338_Tucson:FA_HighSpeed_1bit{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Comparing: ENGR338_Tucson:FA_HighSpeed_8bit{sch} with: ENGR338_Tucson:FA_HighSpeed_8bit{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.0 seconds.
```