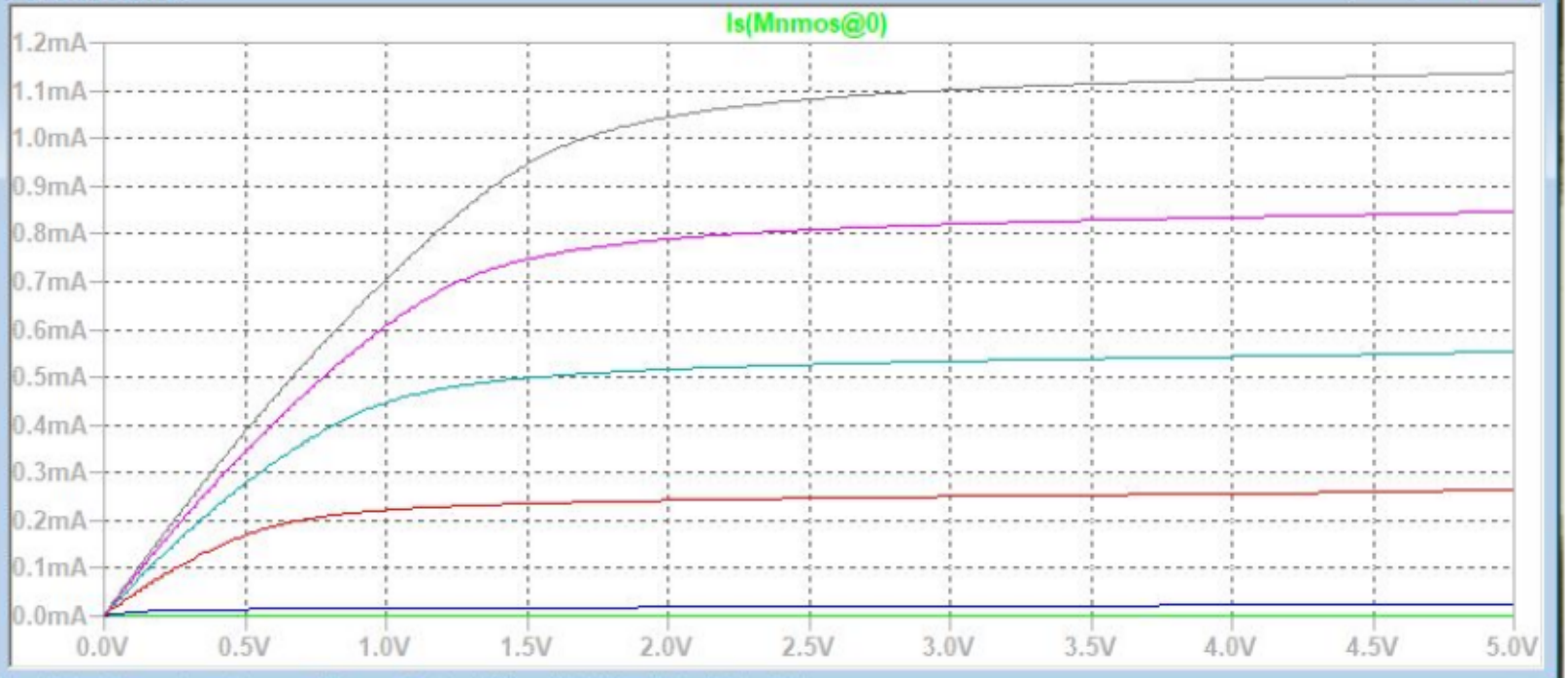
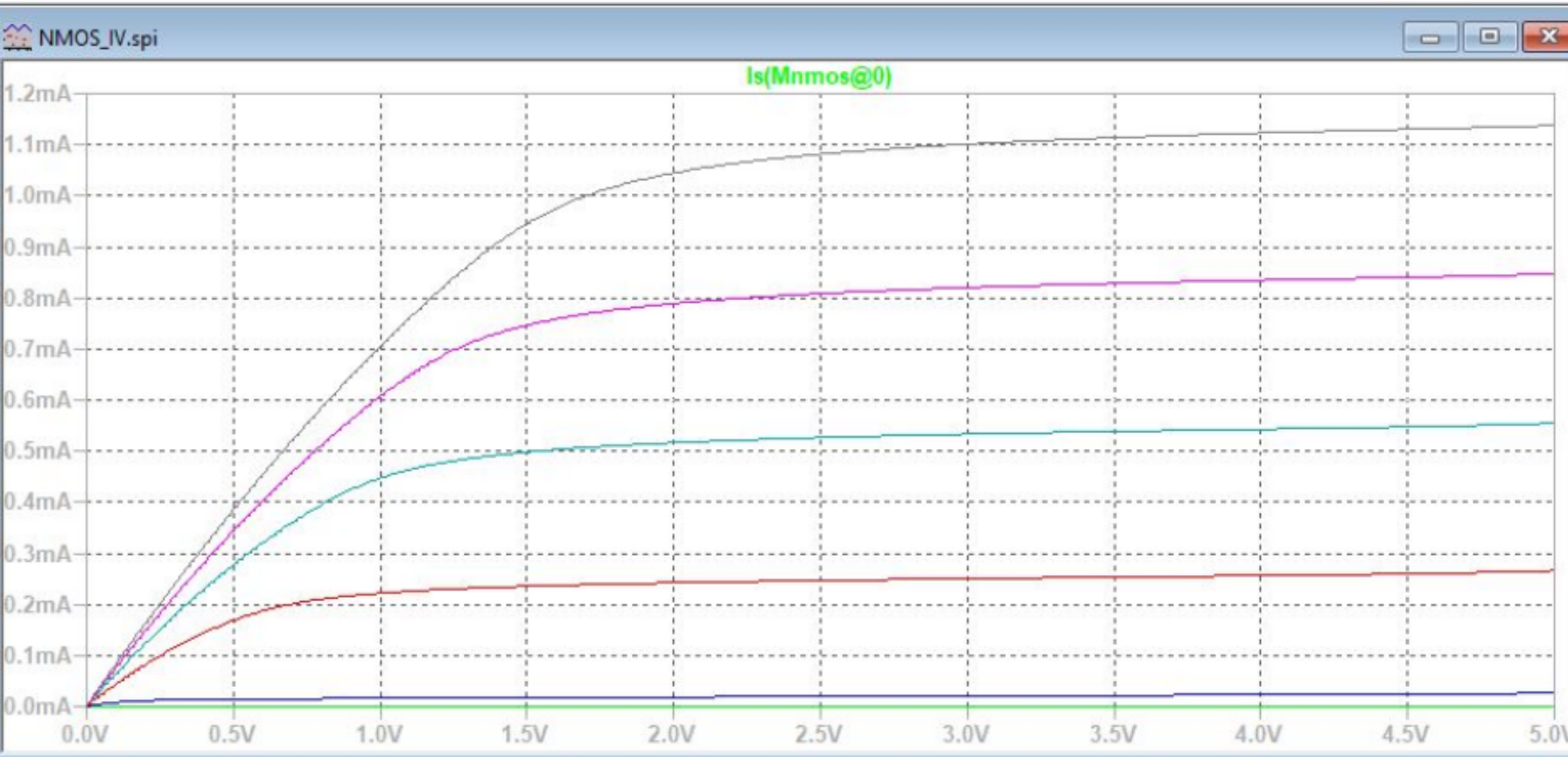
NMOS_IV.spi

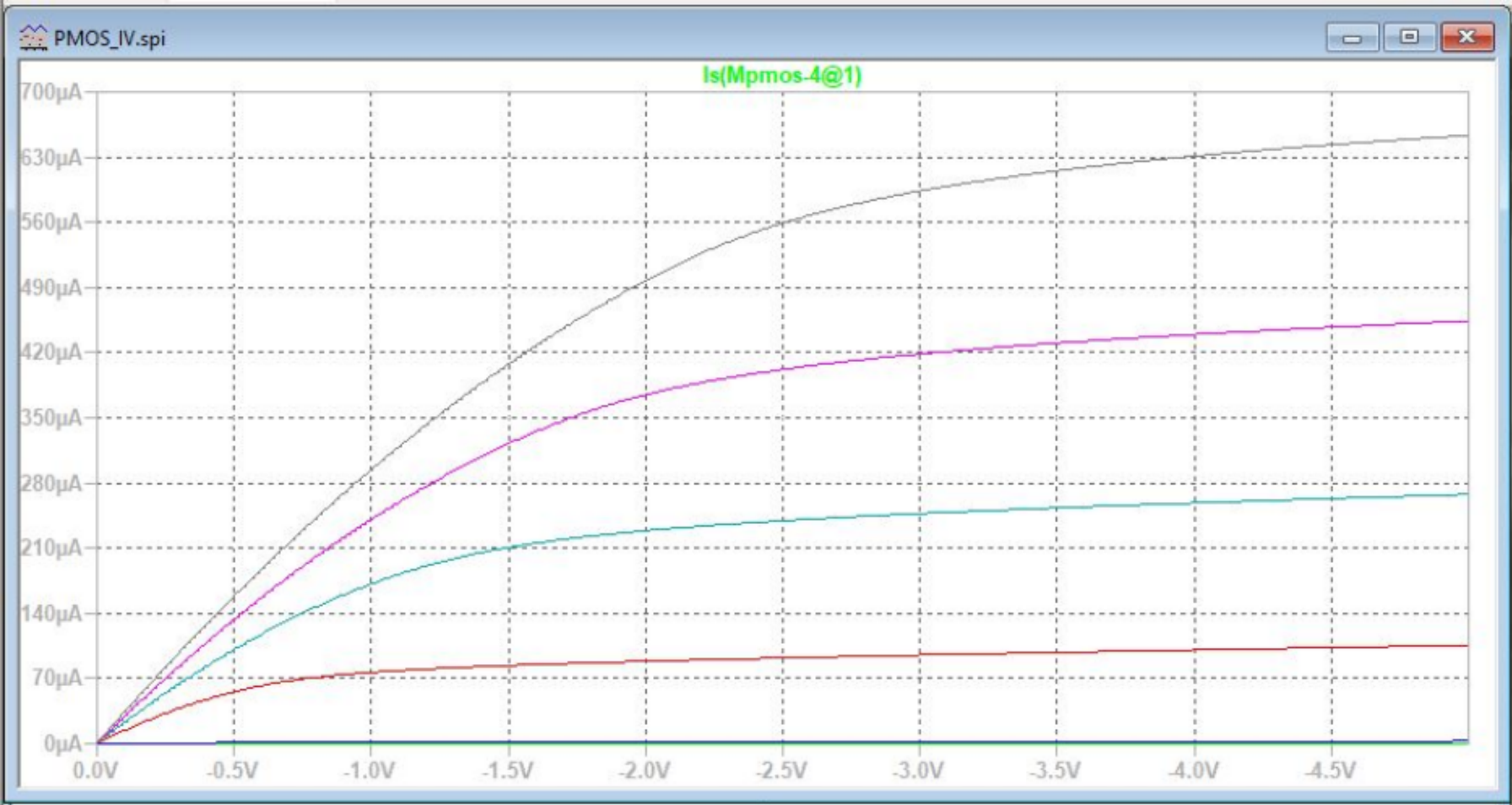



```
*** Created on Tue Feb 23, 2021 12:19:30
*** Last revised on Mon Mar 01, 2021 20:07:23
*** Written on Mon Mar 01, 2021 20:07:43 by Electric VLSI Design System, ver
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** TOP LEVEL CELL: NMOS_IV{lay}
Mnmos@0 s g d gnd NMOS L=0.6U W=3U AS=6.75P AD=6.75P PS=10.5U PD=10.5U

* Spice Code nodes in cell cell 'NMOS_IV{lay}'
vs s 0 DC 0
vw w 0 DC 0
vg g 0 DC 0
vd d 0 DC 0
.dc vd 0 5 1m vg 0 5 1
.include F:\spring21\ENGR338_digitalElectronics\Lab4\C5_models.txt
.END
```




```
*** SPICE deck for cell NMOS_IV{sch} from library ENGR338_Tucson
*** Created on Tue Feb 23, 2021 11:44:56
*** Last revised on Mon Mar 01, 2021 20:43:30
*** Written on Mon Mar 01, 2021 20:46:01 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

.global gnd

*** TOP LEVEL CELL: NMOS_IV{sch}
Mnmos@0 s g d gnd NMOS L=0.6U W=3U

* Spice Code nodes in cell cell 'NMOS_IV{sch}'
vs s 0 DC 0
vw w 0 DC 0
vg g 0 DC 0
vd d 0 DC 0
.dc vd 0 5 1m vg 0 5 1
.include F:\spring21\ENGR338_digitalElectronics\Lab4\C5_models.txt
.END
```


```
*** SPICE deck for cell PMOS_IV{lay} from library ENGR338_Tucson
*** Created on Tue Feb 23, 2021 12:19:38
*** Last revised on Mon Mar 01, 2021 20:04:16
*** Written on Mon Mar 01, 2021 20:47:17 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
*** WARNING: no power connection for P-transistor wells in cell 'PMOS_IV{lay}'

*** TOP LEVEL CELL: PMOS_IV{lay}
Mpmos@0 d g s vdd PMOS L=0.6U W=3U AS=6.75P AD=6.75P PS=10.5U PD=10.5U

* Spice Code nodes in cell cell 'PMOS_IV{lay}'
vs s 0 DC 0
vw w 0 DC 0
vg g 0 DC 0
vd d 0 DC 0
.dc vd 0 -5 -1m vg 0 -5 -1
.include F:\spring21\ENGR338_digitalElectronics\Lab4\C5_models.txt
.END
```




```
*** SPICE deck for cell PMOS_IV{sch} from library ENGR338_Tucson
*** Created on Tue Feb 23, 2021 12:02:34
*** Last revised on Mon Mar 01, 2021 20:48:09
*** Written on Mon Mar 01, 2021 20:48:20 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
*** WARNING: no power connection for P-transistor wells in cell 'PMOS_IV{sch}'

*** TOP LEVEL CELL: PMOS_IV{sch}
Mpmos-4@1 d g s w PMOS L=0.6U W=3U

* Spice Code nodes in cell cell 'PMOS_IV{sch}'
vs s 0 DC 0
vw w 0 DC 0
vg g 0 DC 0
vd d 0 DC 0
.dc vd 0 -5 -1m vg 0 -5 -1
.include F:\spring21\ENGR338_digitalElectronics\Lab4\C5_models.txt
.END
```