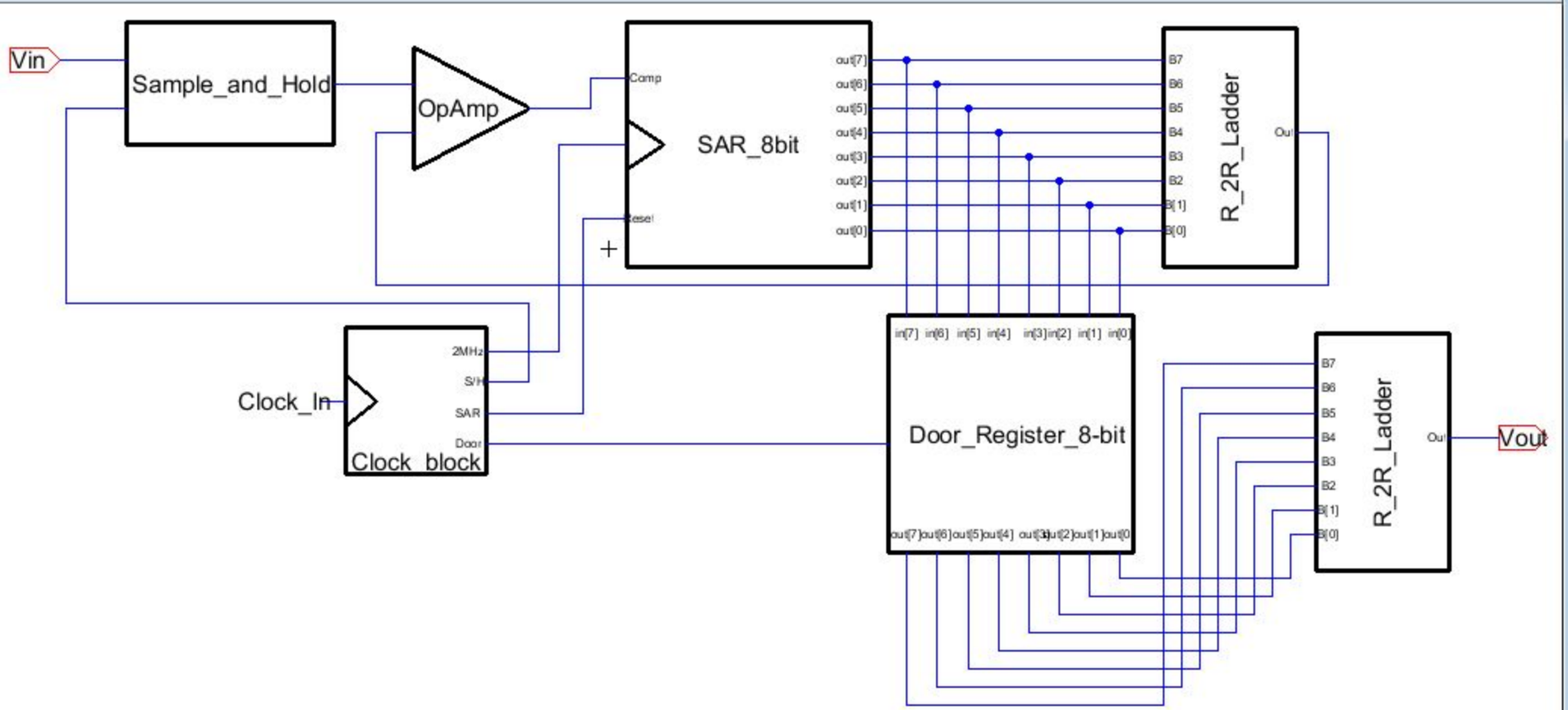


```
==================================572==================
Checking schematic cell 'AND_50nmEQ{sch}'
   No errors found
Checking schematic cell 'NAND_3input{sch}'
   No errors found
Checking schematic cell 'DFlipFlop_TI{sch}'
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Checking schematic cell 'Inverter_40_20{sch}'
   No errors found
Checking schematic cell 'NAND_2input_50nmEQ{sch}'
   No errors found
Checking schematic cell 'Clock_block{sch}'
   No errors found
Checking schematic cell 'Comparator{sch}'
   No errors found
Checking schematic cell 'Door_Register_8-bit{sch}'
   No errors found
Checking schematic cell 'R_2R_Ladder_8bit{sch}'
   No errors found
Checking schematic cell 'Buffer{sch}'
   No errors found
Checking schematic cell 'SAR_8bit{sch}'
   No errors found
Checking schematic cell 'Sample_and_Hold{sch}'
   No errors found
Checking schematic cell 'ADC_SAR_8bit{sch}'
   No errors found
```

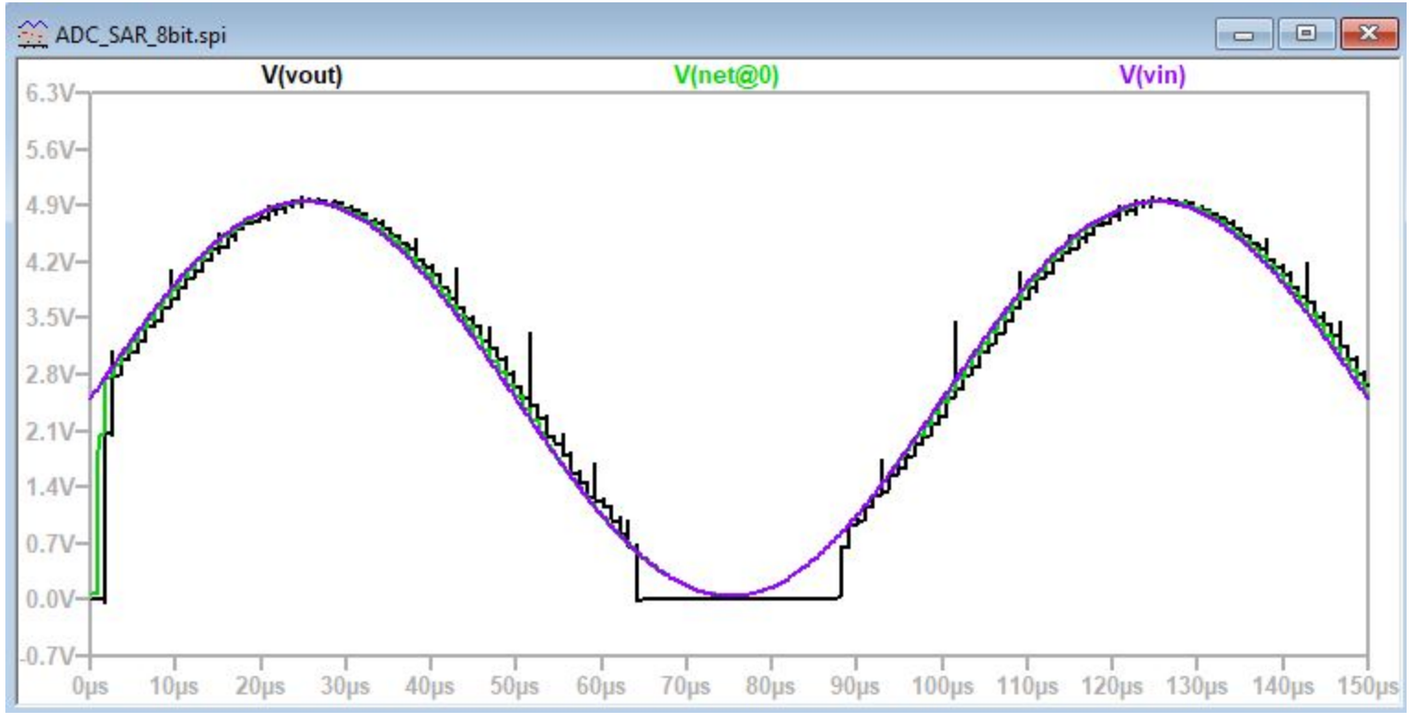
ADC_SAR_8bit.spi
V(vout)
V(net@0)
V(vin)
6.3V
5.6V
4.9V
4.2V
3.5V
2.8V
2.1V
1.4V
0.7V
0.0V
-0.7V
0µs
10µs
20µs
30µs
40µs
50µs
60µs
70µs
80µs
90µs
100µs
110µs
120µs
130µs
140µs
150µs