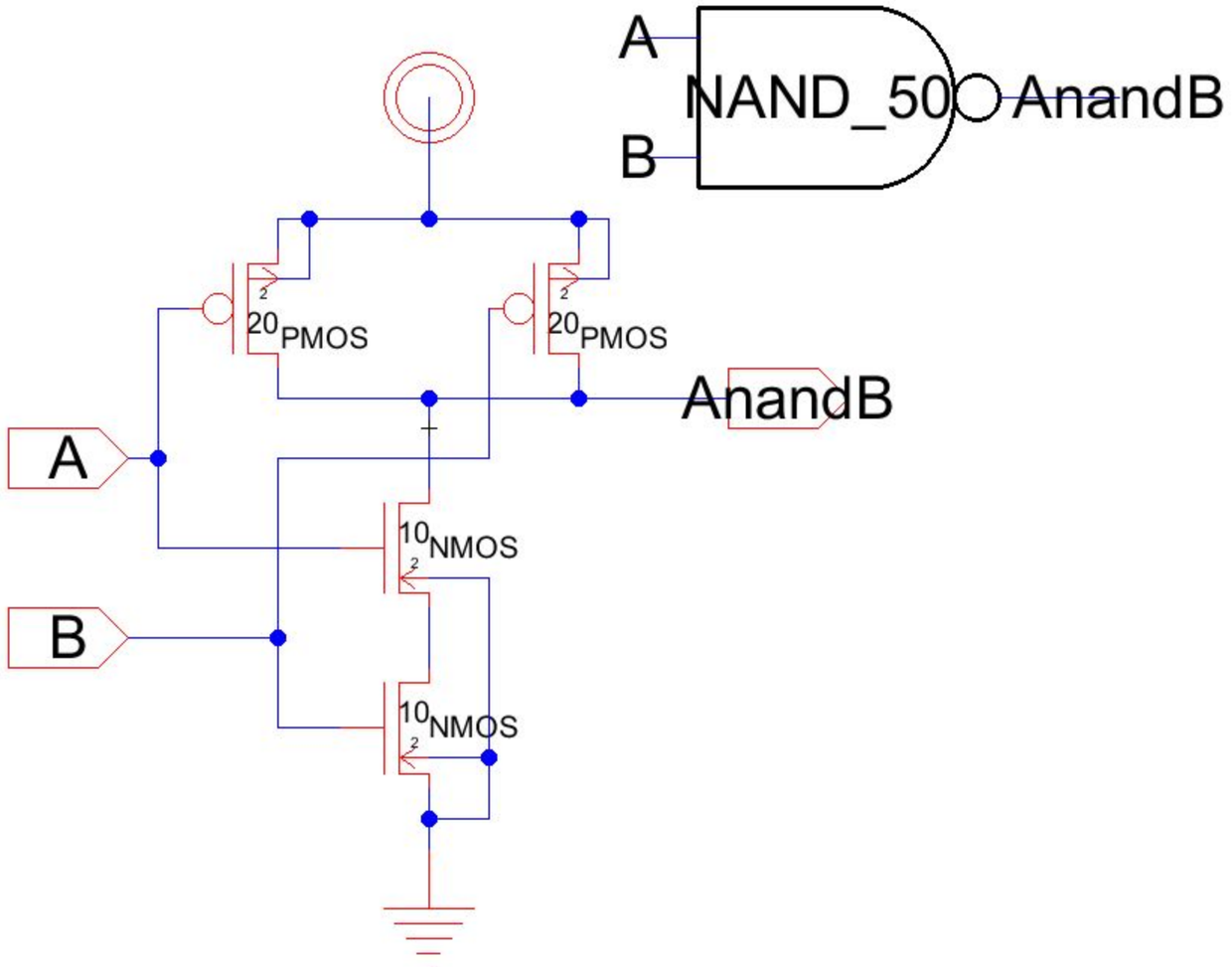
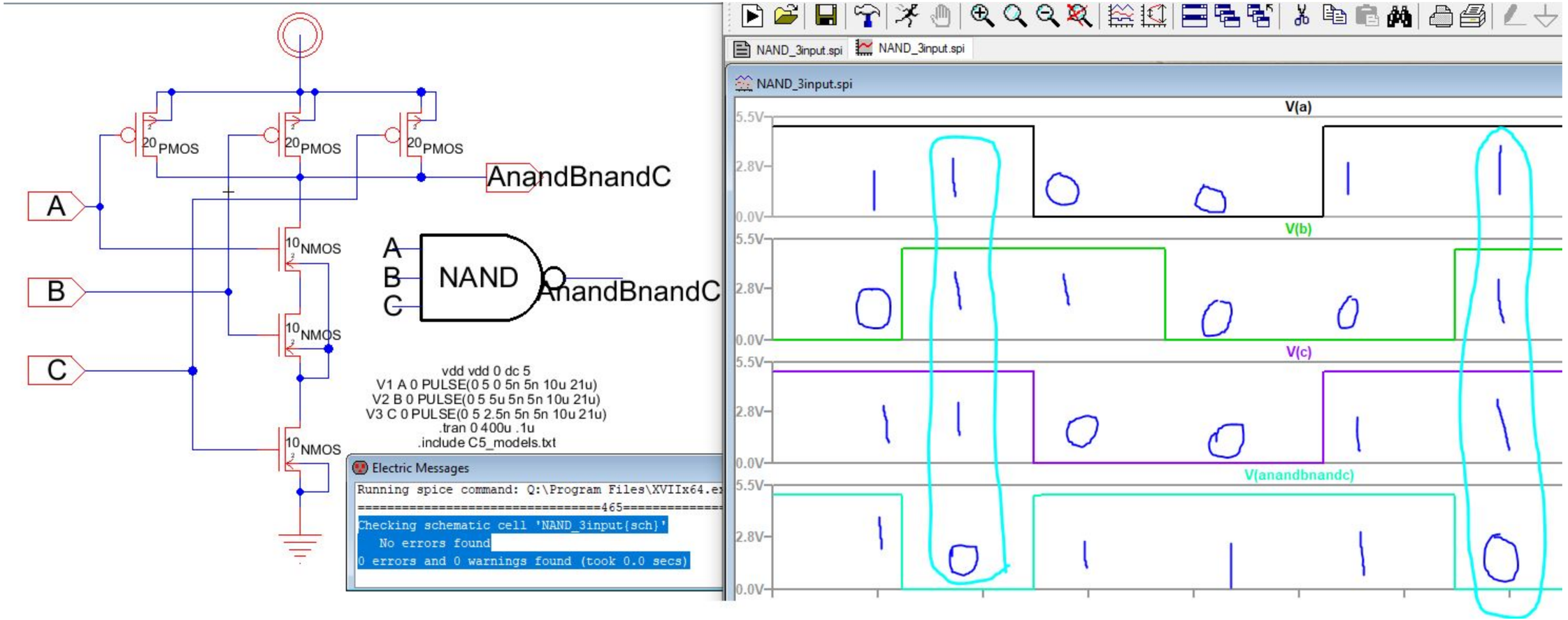
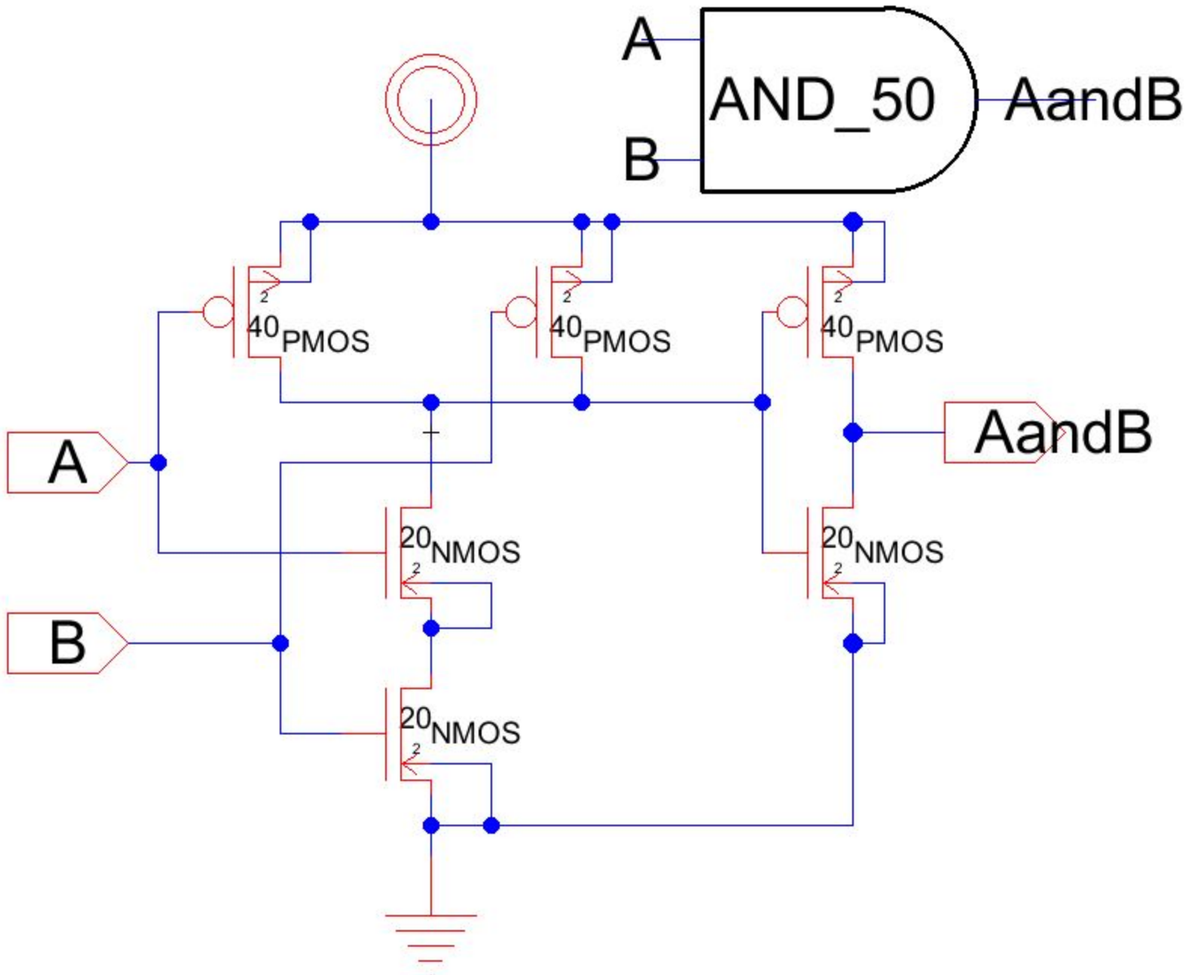
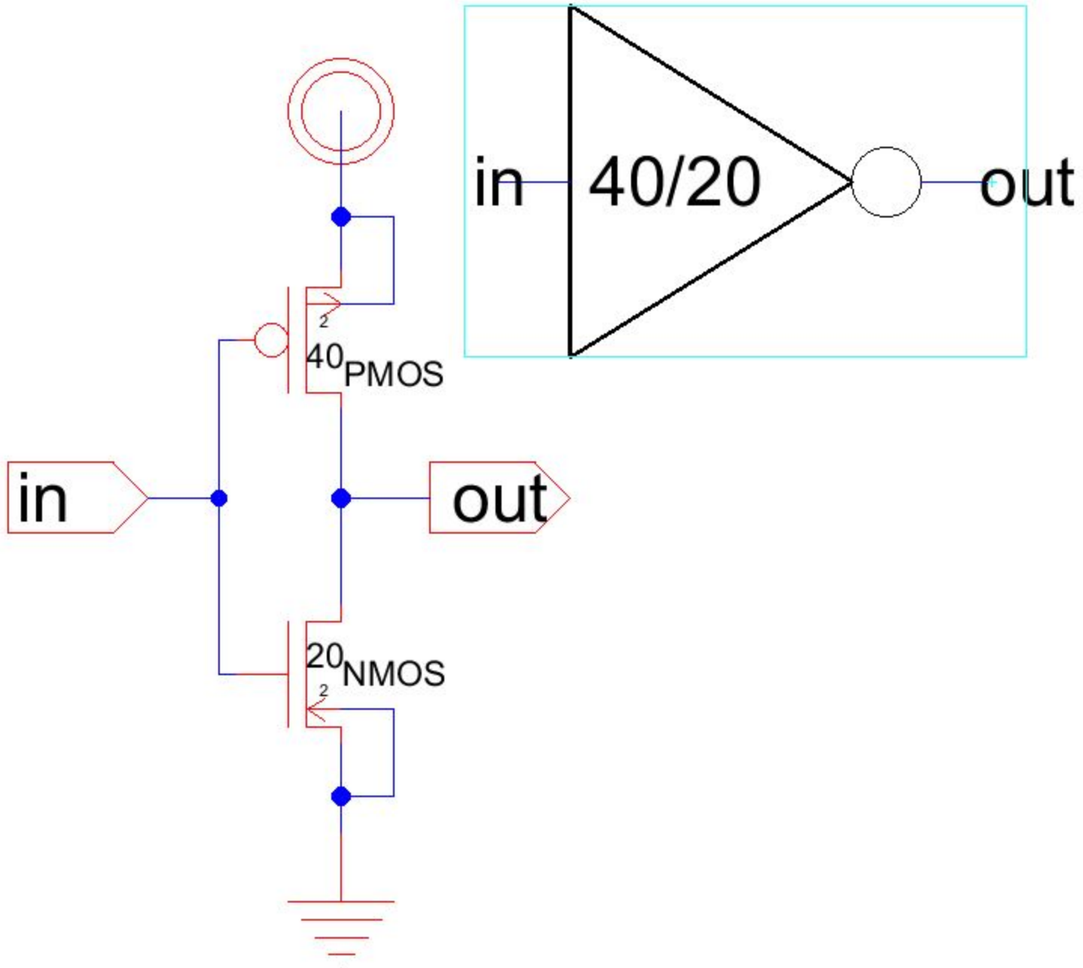
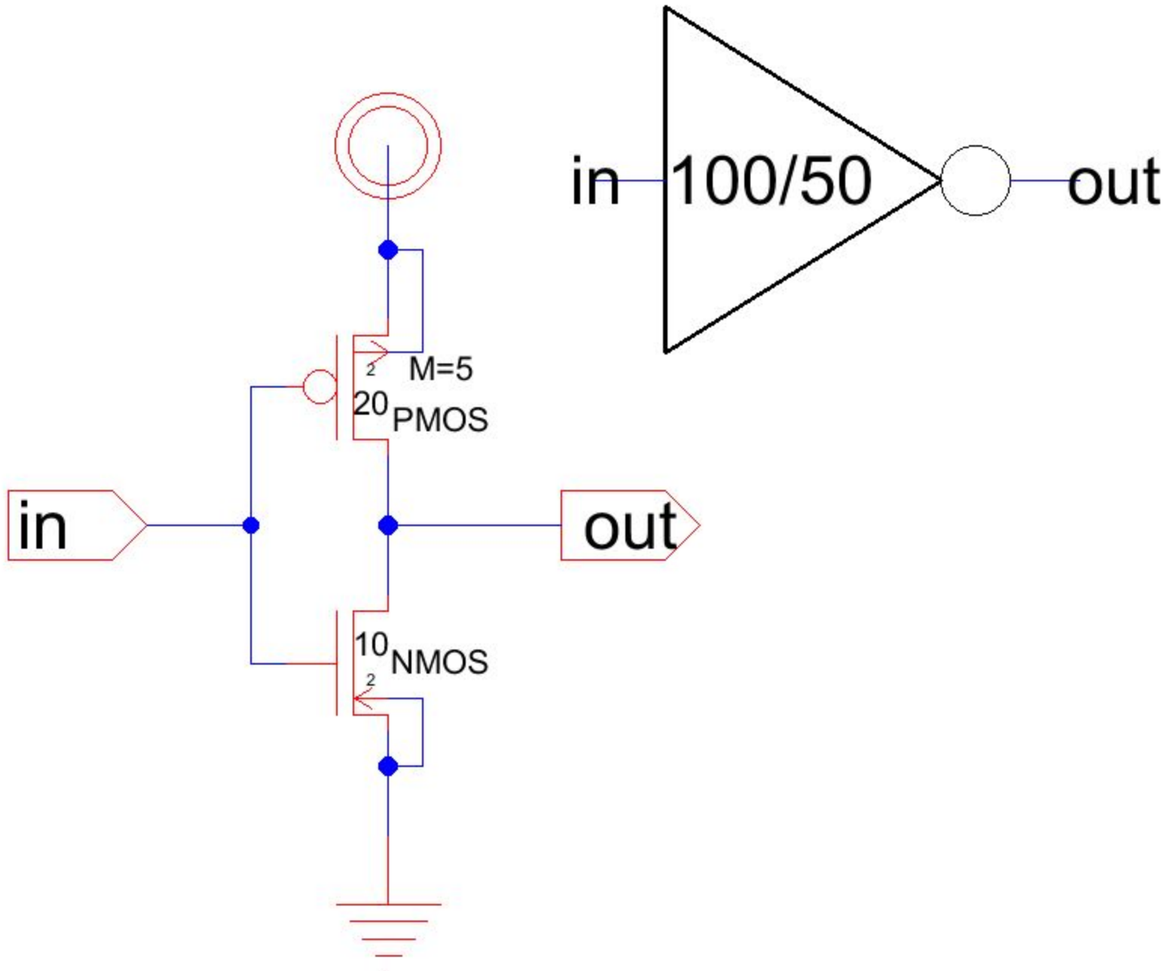
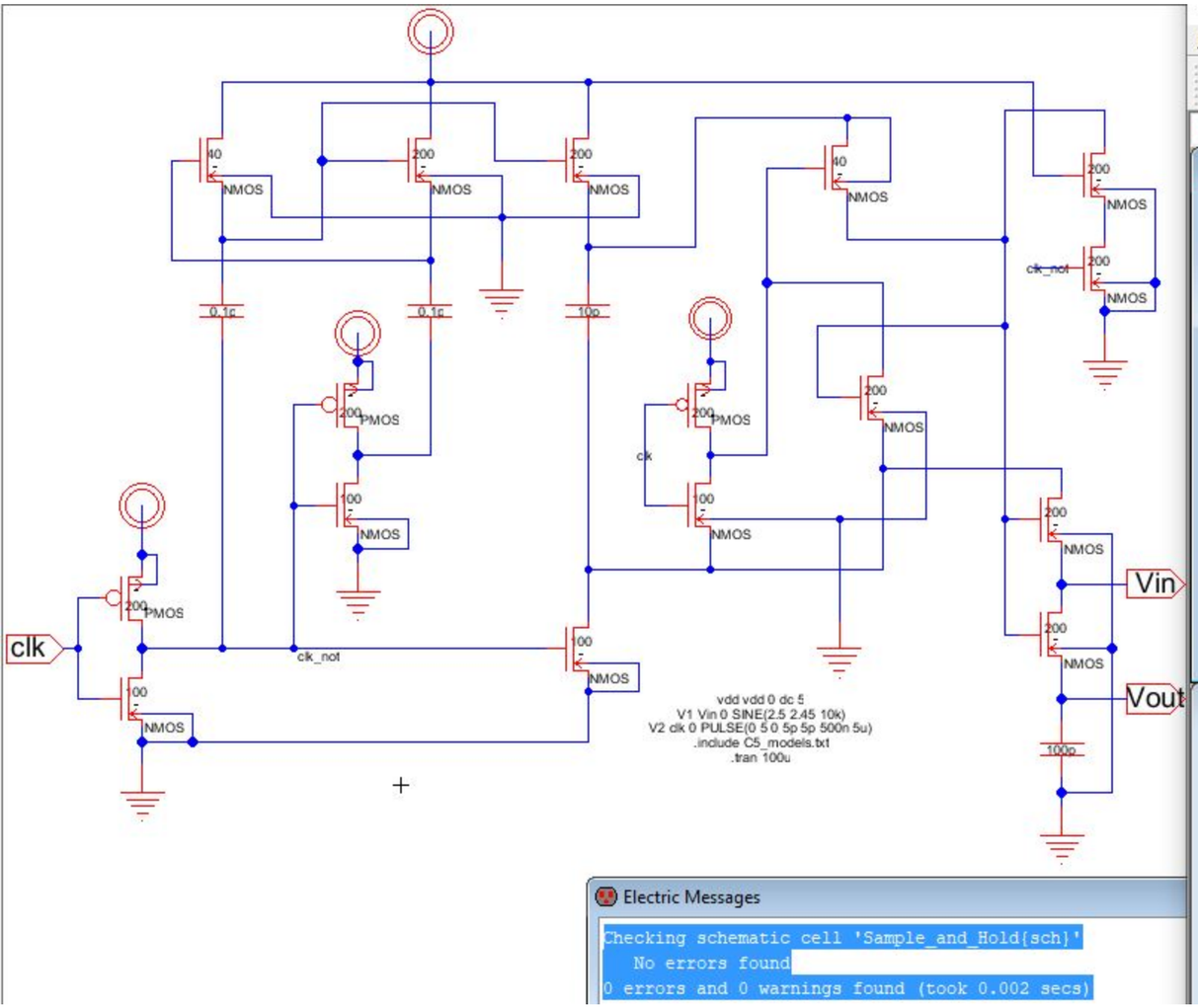

A
B
NAND_50
AnandB
20PMOS
20PMOS
AnandB
A
10NMOS
B
10NMOS


20 PMOS
20 PMOS
20 PMOS
AnandBnandC
A
B
C
10 NMOS
10 NMOS
10 NMOS
A
B
C
NAND
AnandBnandC
vdd vdd 0 dc 5
V1 A 0 PULSE(0 5 0 5n 5n 10u 21u)
V2 B 0 PULSE(0 5 5u 5n 5n 10u 21u)
V3 C 0 PULSE(0 5 2.5n 5n 5n 10u 21u)
.tran 0 400u .1u
.include C5_models.txt
Electric Messages
Running spice command: Q:\Program Files\XVIIx64.ex
Checking schematic cell 'NAND_3input{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)
NAND_3input.spi
NAND_3input.spi
NAND_3input.spi
V(a)
V(b)
V(c)
V(anandbnandc)
5.5V
2.8V
0.0V


A
B
AND_50
AandB
40PMOS
40PMOS
40PMOS
A
B
AandB
20NMOS
20NMOS
20NMOS


in
40/20
out
2
40PMOS
in
out
20NMOS
2


in
100/50
out
M=5
20
PMOS
in
out
10
NMOS

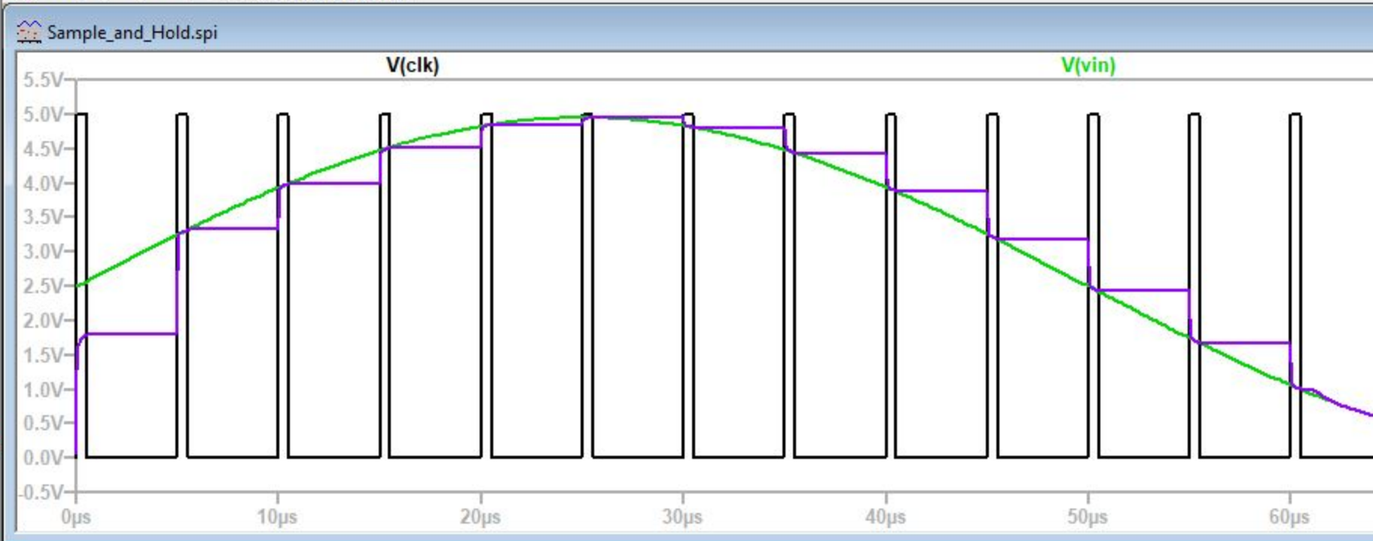


Electric Messages

```
Checking schematic cell 'Sample_and_Hold{sch}'
   No errors found
0 errors and 0 warnings found (took 0.002 secs)
```

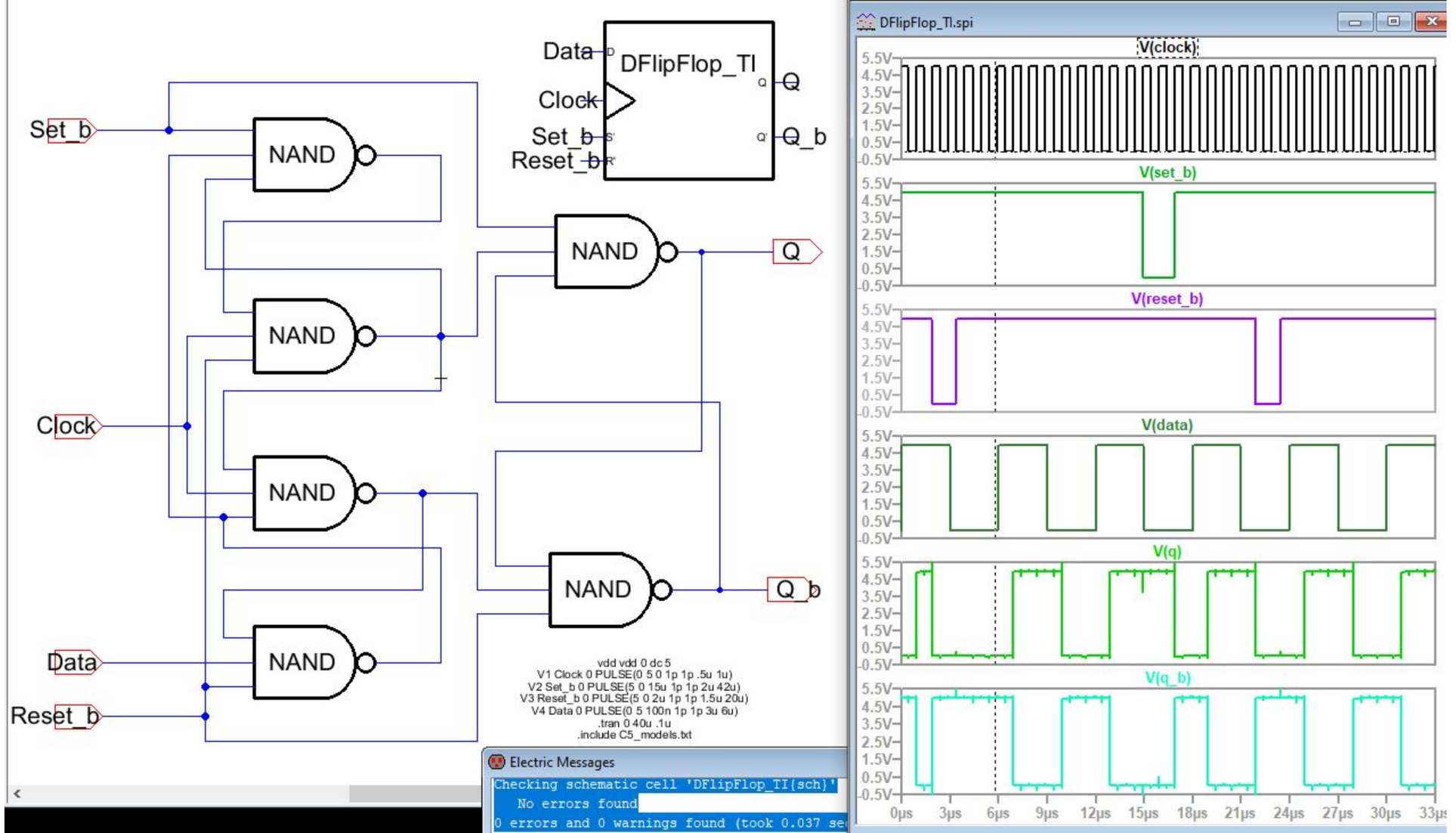
File View Plot Settings Simulation Tools Window Help

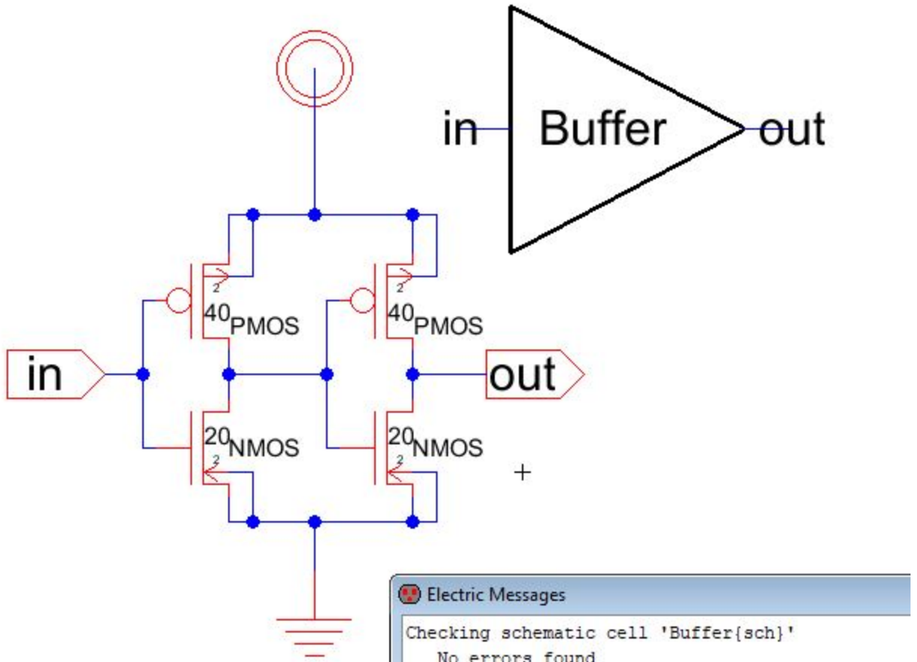
Sample_and_Hold.spi Sample_and_Hold.spi

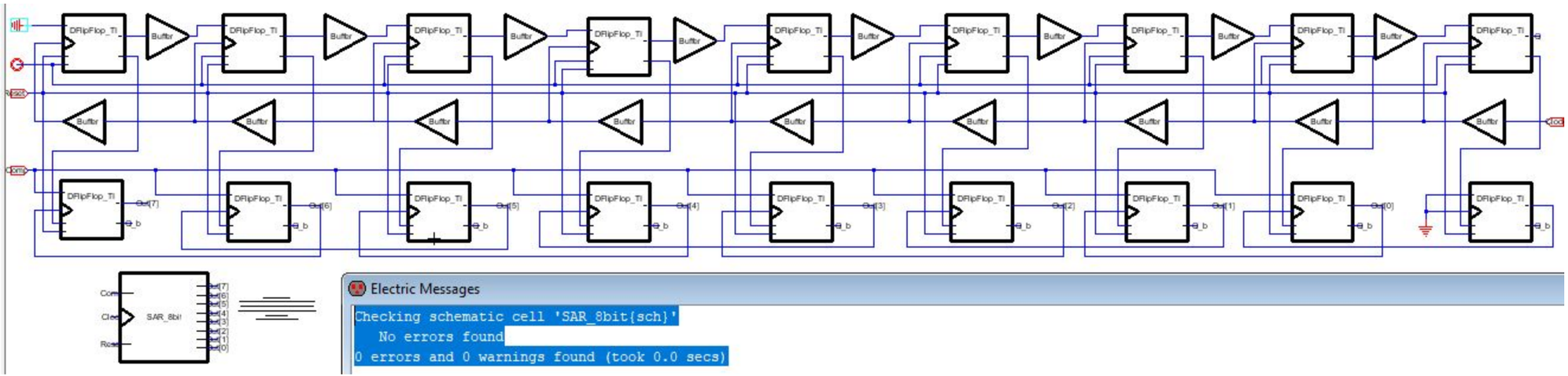


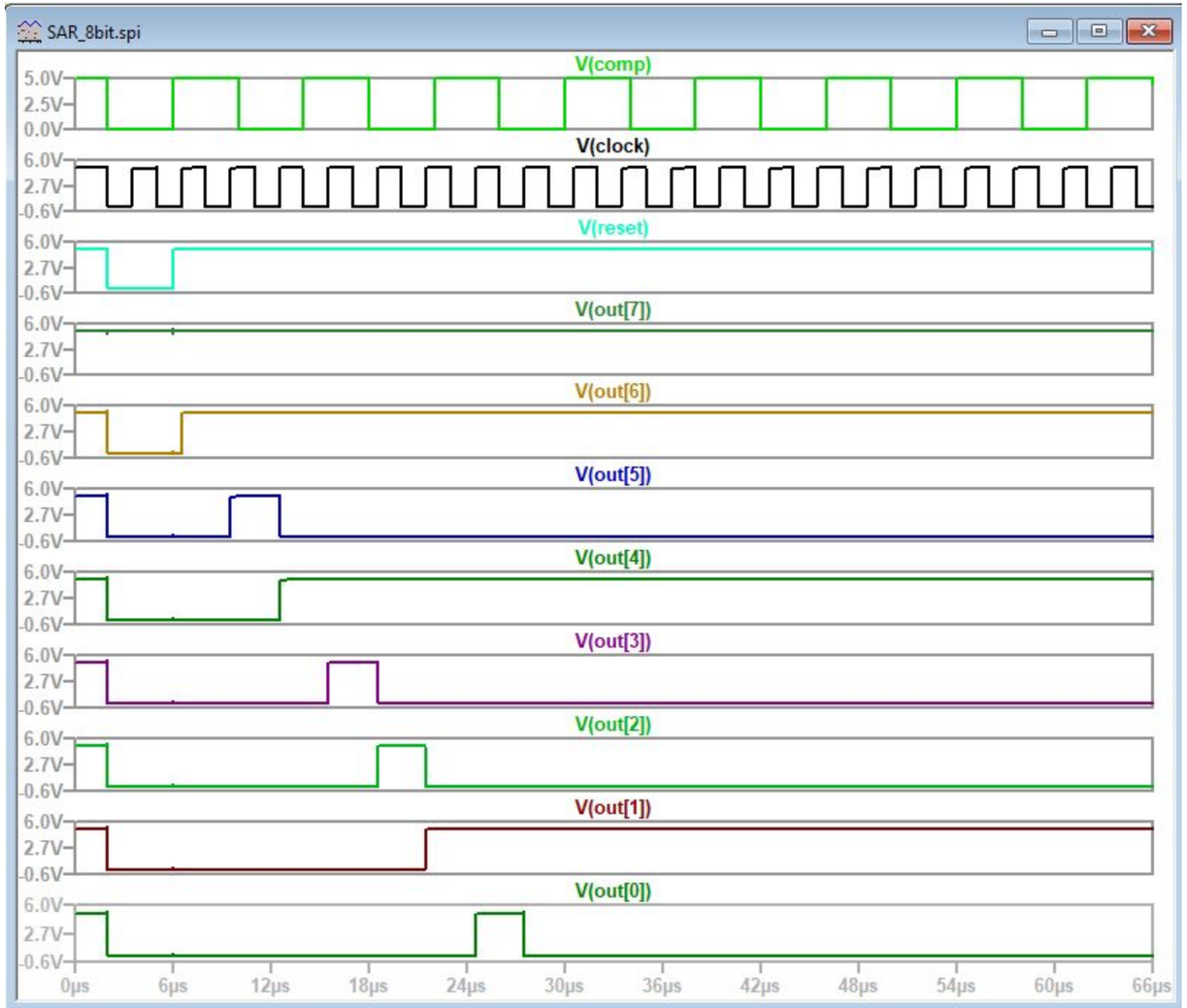
Sample_and_Hold.spi

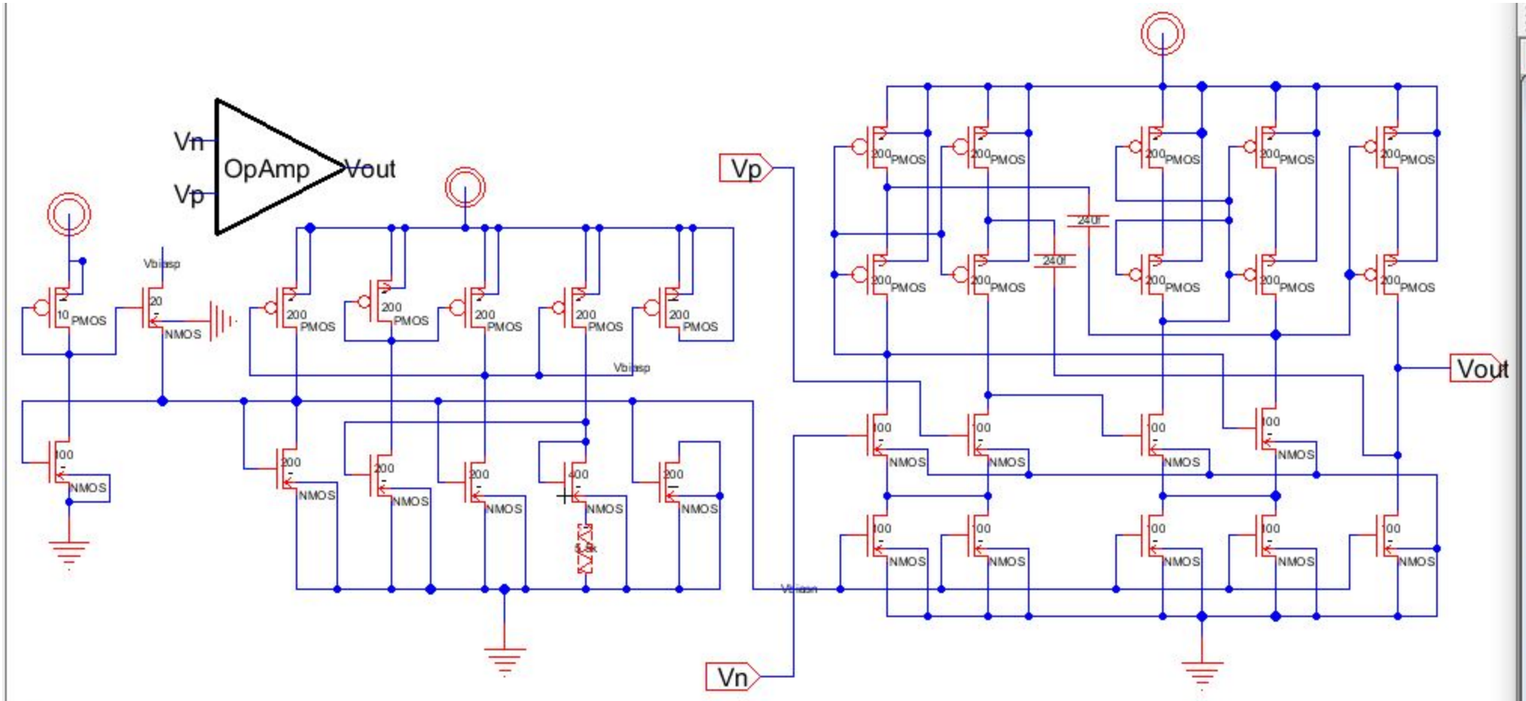
```
*** SPICE deck for cell Sample_and_Hold{sch} from library ENGR338_Tucson
*** Created on Sun Dec 05, 2021 03:02:27
*** Last revised on Tue Dec 07, 2021 20:26:28
*** Written on Tue Dec 07, 2021 20:26:39 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

.global gnd vdd

*** TOP LEVEL CELL: Sample_and_Hold{sch}
```


Data
DFlipFlop_TI
Clock
Set_b
Reset_b
Q
Q_b
Set_b
NAND
NAND
NAND
NAND
NAND
NAND
Clock
Data
Reset_b
Q
Q_b
vdd vdd 0 dc 5
V1 Clock 0 PULSE(0 5 0 1p 1p .5u 1u)
V2 Set_b 0 PULSE(5 0 15u 1p 1p 2u 42u)
V3 Reset_b 0 PULSE(5 0 2u 1p 1p 1.5u 20u)
V4 Data 0 PULSE(0 5 100n 1p 1p 3u 6u)
.tran 0 40u .1u
.include C5_models.txt
Electric Messages
Checking schematic cell 'DFlipFlop_TI{sch}'
No errors found
0 errors and 0 warnings found (took 0.037 se
DFlipFlop_TI.spi
V(clock)
V(set_b)
V(reset_b)
V(data)
V(q)
V(q_b)
5.5V
4.5V
3.5V
2.5V
1.5V
0.5V
-0.5V
0µs
3µs
6µs
9µs
12µs
15µs
18µs
21µs
24µs
27µs
30µs
33µs


in
Buffer
out
40PMOS
40PMOS
in
out
20NMOS
20NMOS
Electric Messages
Checking schematic cell 'Buffer{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)

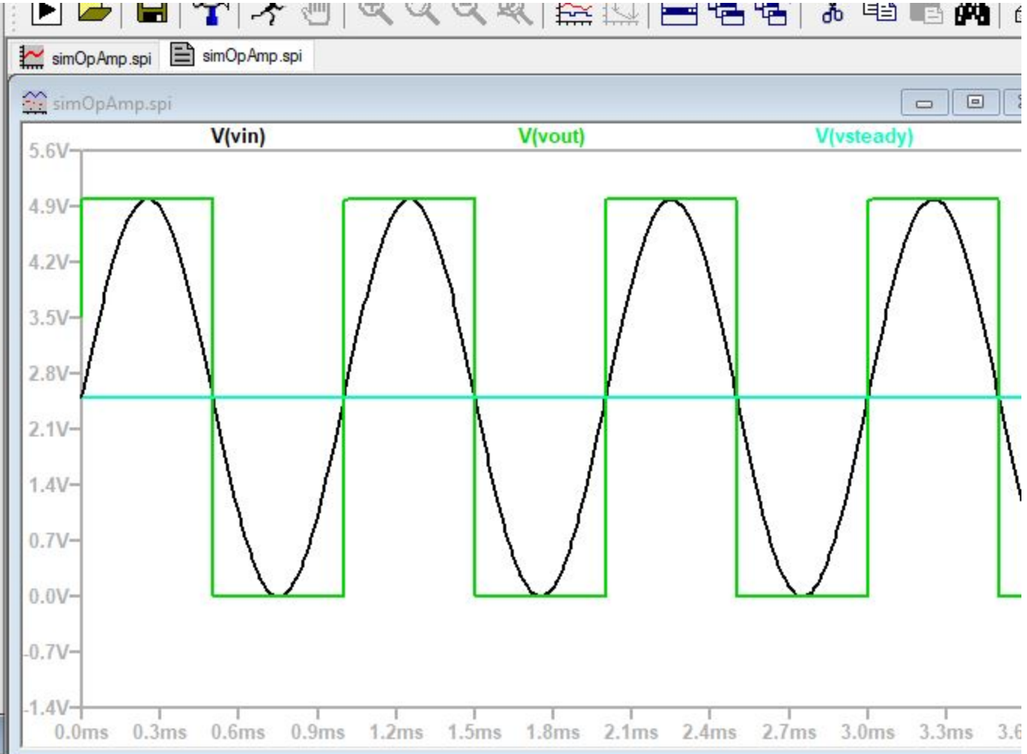

DFlipFlop_TI
Buffbr
SAR_8bit
Electric Messages
Checking schematic cell 'SAR_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)


SAR_8bit.spi
V(comp)
5.0V
2.5V
0.0V
V(clock)
6.0V
2.7V
-0.6V
V(reset)
V(out[7])
V(out[6])
V(out[5])
V(out[4])
V(out[3])
V(out[2])
V(out[1])
V(out[0])
0µs
6µs
12µs
18µs
24µs
30µs
36µs
42µs
48µs
54µs
60µs
66µs



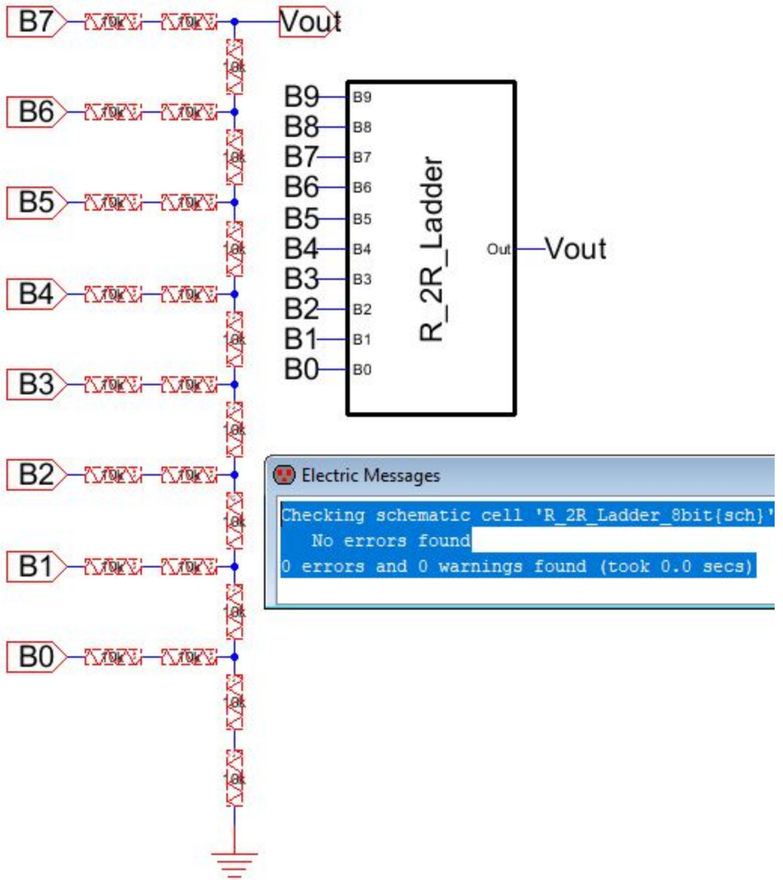
Electric Messages

```
Moved node OpAmp{ic}[OpAmp@0] by (1,-0.5)
================================262================================
Checking schematic cell 'OpAmp{sch}'
   No errors found
0 errors and 0 warnings found (took 0.016 secs)
```



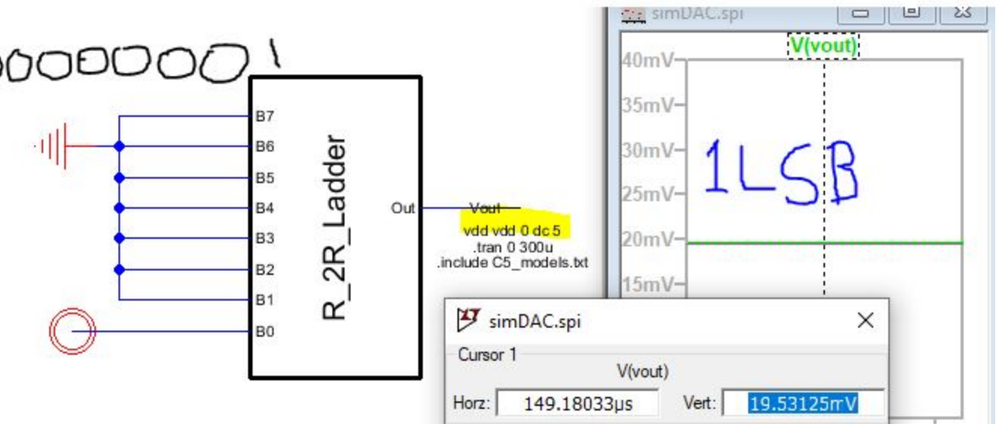
simOpAmp.spi

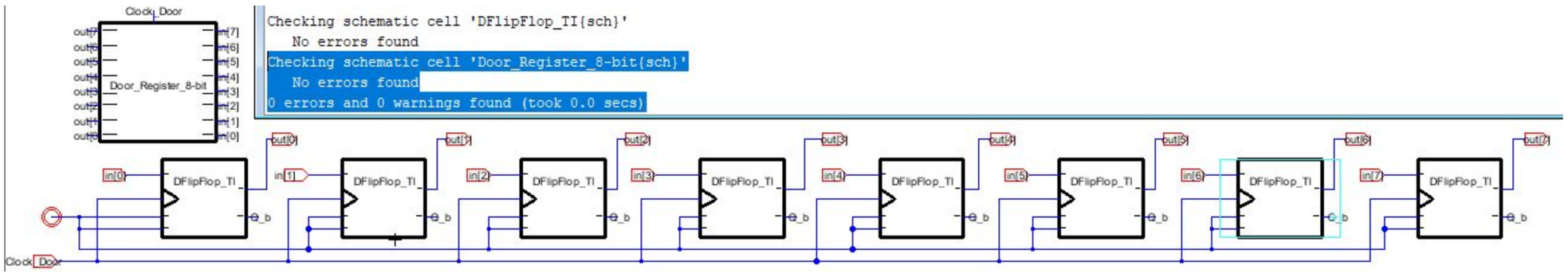
```
*** SUBCIRCUIT ENGR338_Tucson_finalProgress_ OpAmp FROM CELL OpAmp
.SUBCKT ENGR338_Tucson_finalProgress_ OpAmp Vn Vout Vp
```

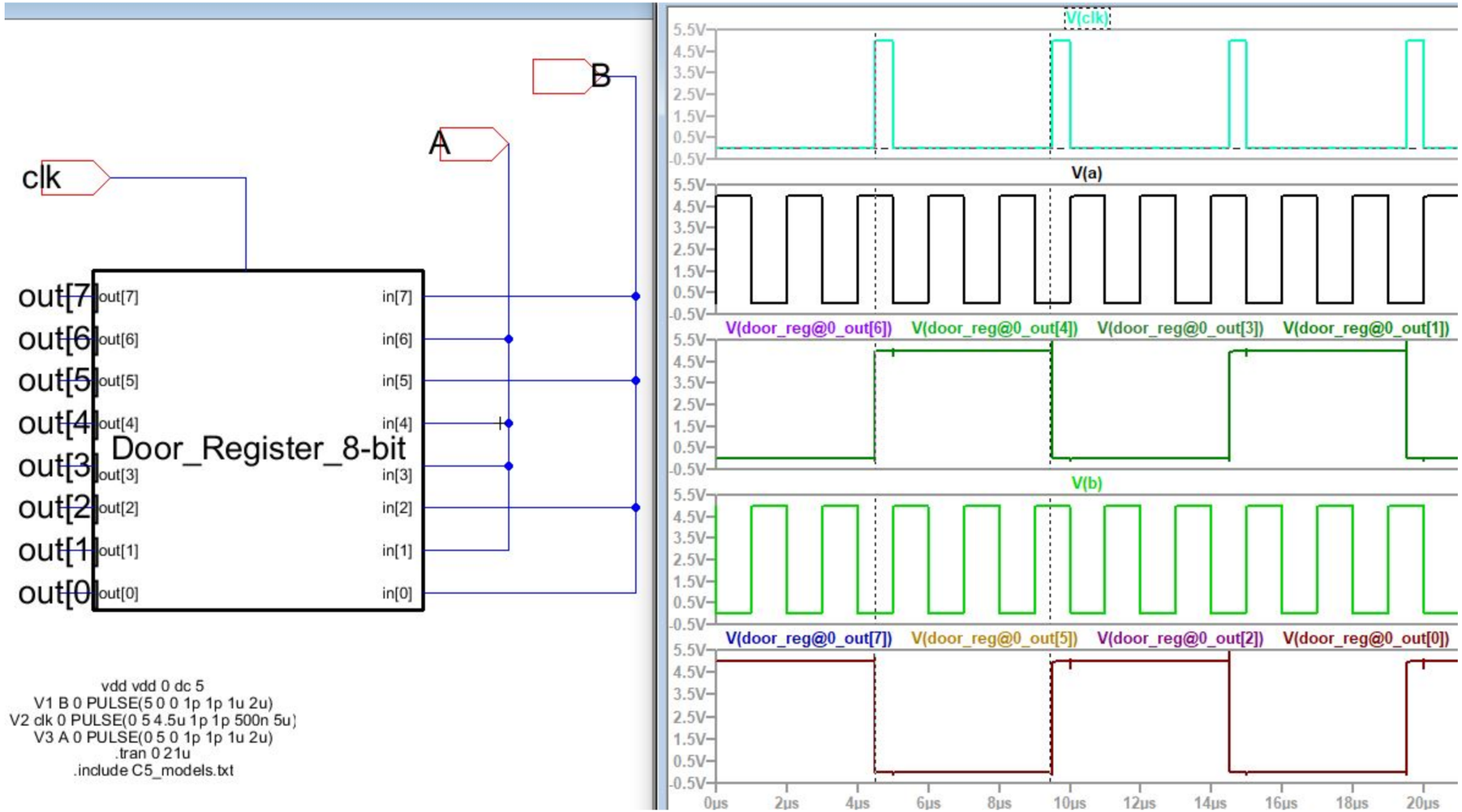

B7
Vout
B6
B5
B4
B3
B2
B1
B0
B9
B8
B7
B6
B5
B4
B3
B2
B1
B0
R_2R_Ladder
Out
Vout
Electric Messages
Checking schematic cell 'R_2R_Ladder_8bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)

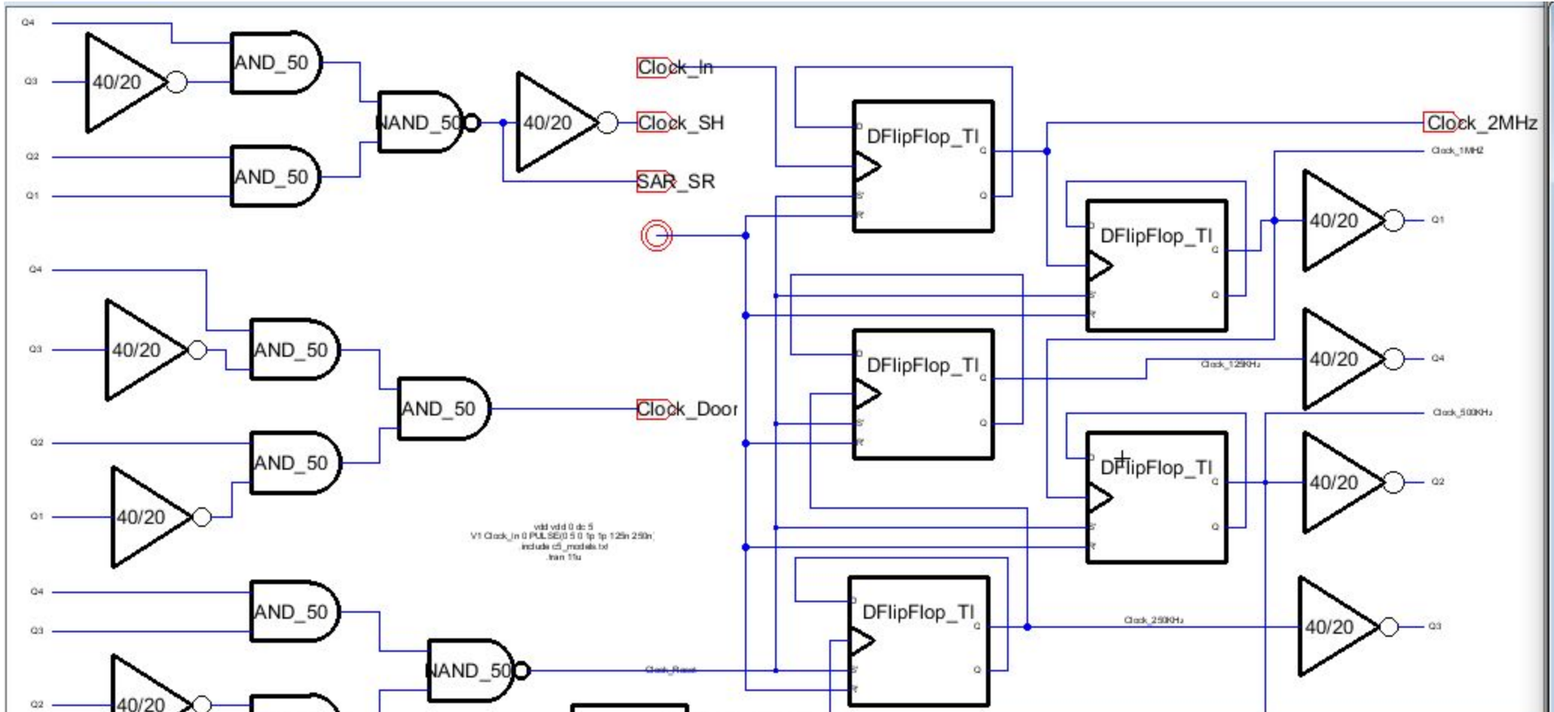
$5V\left(\frac{1}{2^8}\right)=0.0195V$

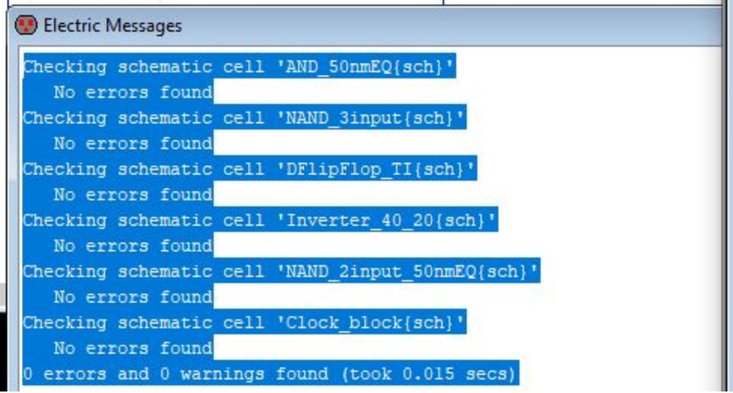
00000001

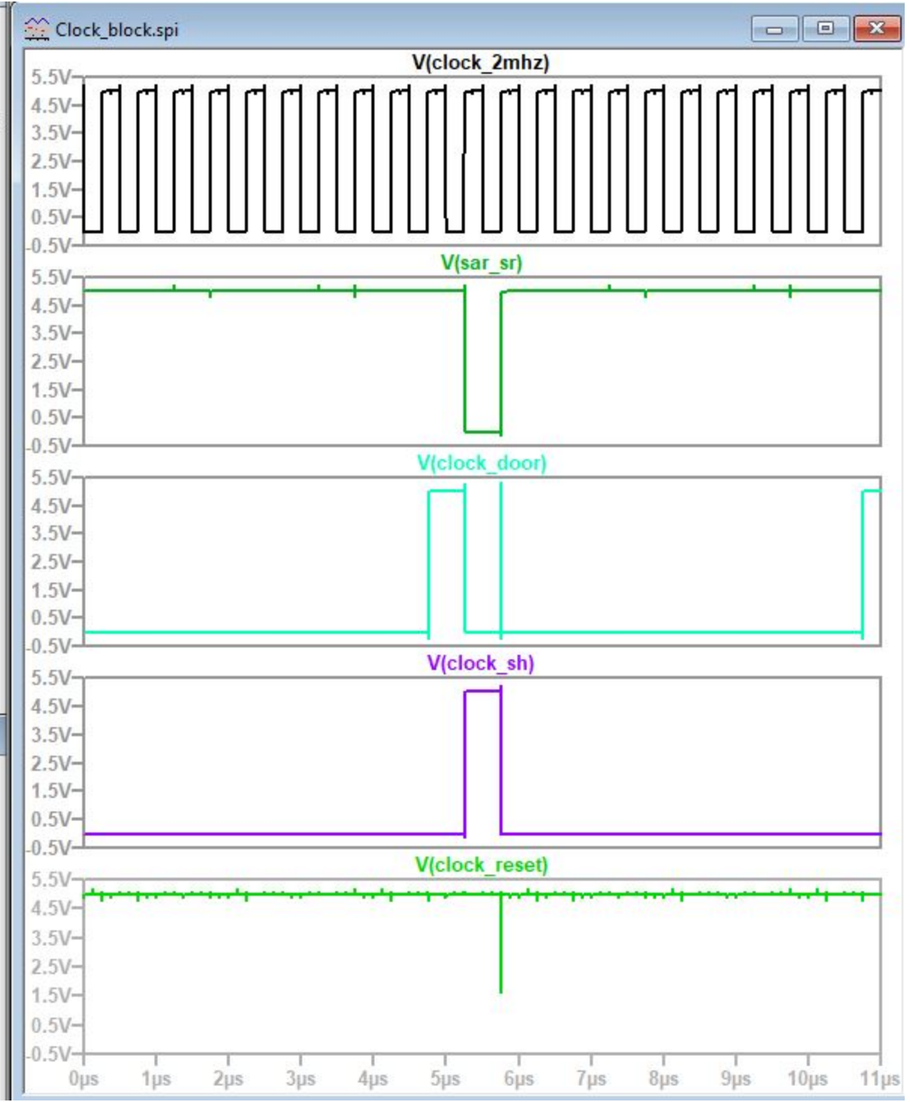



Clock_Door
Door_Register_8-bit
Checking schematic cell 'DFlipFlop_TI{sch}'
No errors found
Checking schematic cell 'Door_Register_8-bit{sch}'
No errors found
0 errors and 0 warnings found (took 0.0 secs)
DFlipFlop_TI
Clock_Door


B
A
clk
out[7]
out[6]
out[5]
out[4]
out[3]
out[2]
out[1]
out[0]
Door_Register_8-bit
in[7]
in[6]
in[5]
in[4]
in[3]
in[2]
in[1]
in[0]
vdd vdd 0 dc 5
V1 B 0 PULSE(5 0 0 1p 1p 1u 2u)
V2 clk 0 PULSE(0 5 4.5u 1p 1p 500n 5u)
V3 A 0 PULSE(0 5 0 1p 1p 1u 2u)
.tran 0 21u
.include C5_models.txt
V(clk)
V(a)
V(door_reg@0_out[6])
V(door_reg@0_out[4])
V(door_reg@0_out[3])
V(door_reg@0_out[1])
V(b)
V(door_reg@0_out[7])
V(door_reg@0_out[5])
V(door_reg@0_out[2])
V(door_reg@0_out[0])
5.5V
4.5V
3.5V
2.5V
1.5V
0.5V
-0.5V
0µs
2µs
4µs
6µs
8µs
10µs
12µs
14µs
16µs
18µs
20µs


Q4
Q3
Q2
Q1
40/20
AND_50
NAND_50
Clock_In
Clock_SH
SAR_SR
DFlipFlop_TI
Clock_2MHz
Clock_1MHz
Clock_128KHz
Clock_500KHz
Clock_250KHz
Clock_Door
Clock_Reset
Clock_block


Electric Messages
Checking schematic cell 'AND_50nmEQ{sch}'
No errors found
Checking schematic cell 'NAND_3input{sch}'
No errors found
Checking schematic cell 'DFlipFlop_TI{sch}'
No errors found
Checking schematic cell 'Inverter_40_20{sch}'
No errors found
Checking schematic cell 'NAND_2input_50nmEQ{sch}'
No errors found
Checking schematic cell 'Clock_block{sch}'
No errors found
0 errors and 0 warnings found (took 0.015 secs)


Clock_block.spi
V(clock_2mhz)
V(sar_sr)
V(clock_door)
V(clock_sh)
V(clock_reset)
5.5V
4.5V
3.5V
2.5V
1.5V
0.5V
-0.5V
0µs
1µs
2µs
3µs
4µs
5µs
6µs
7µs
8µs
9µs
10µs
11µs