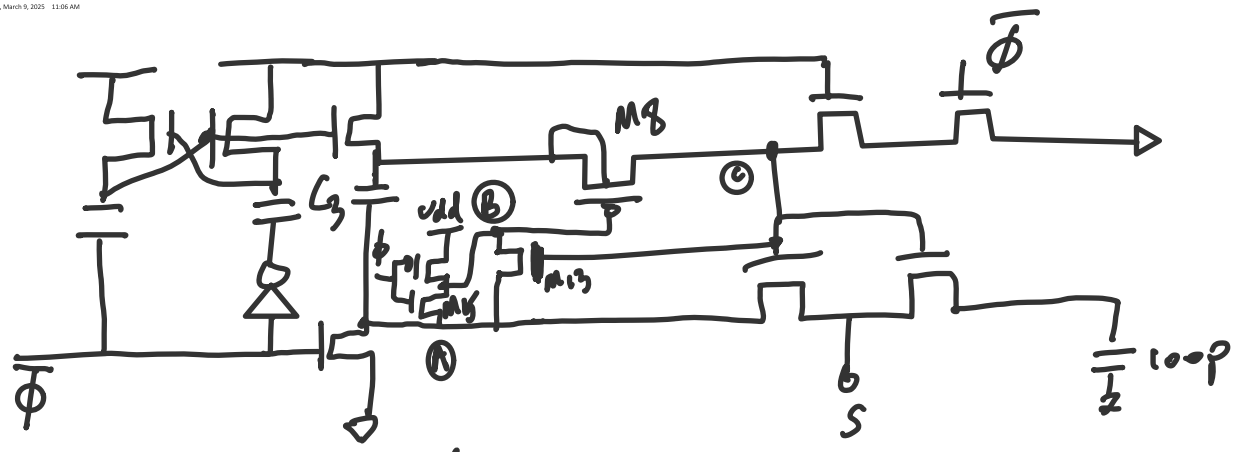
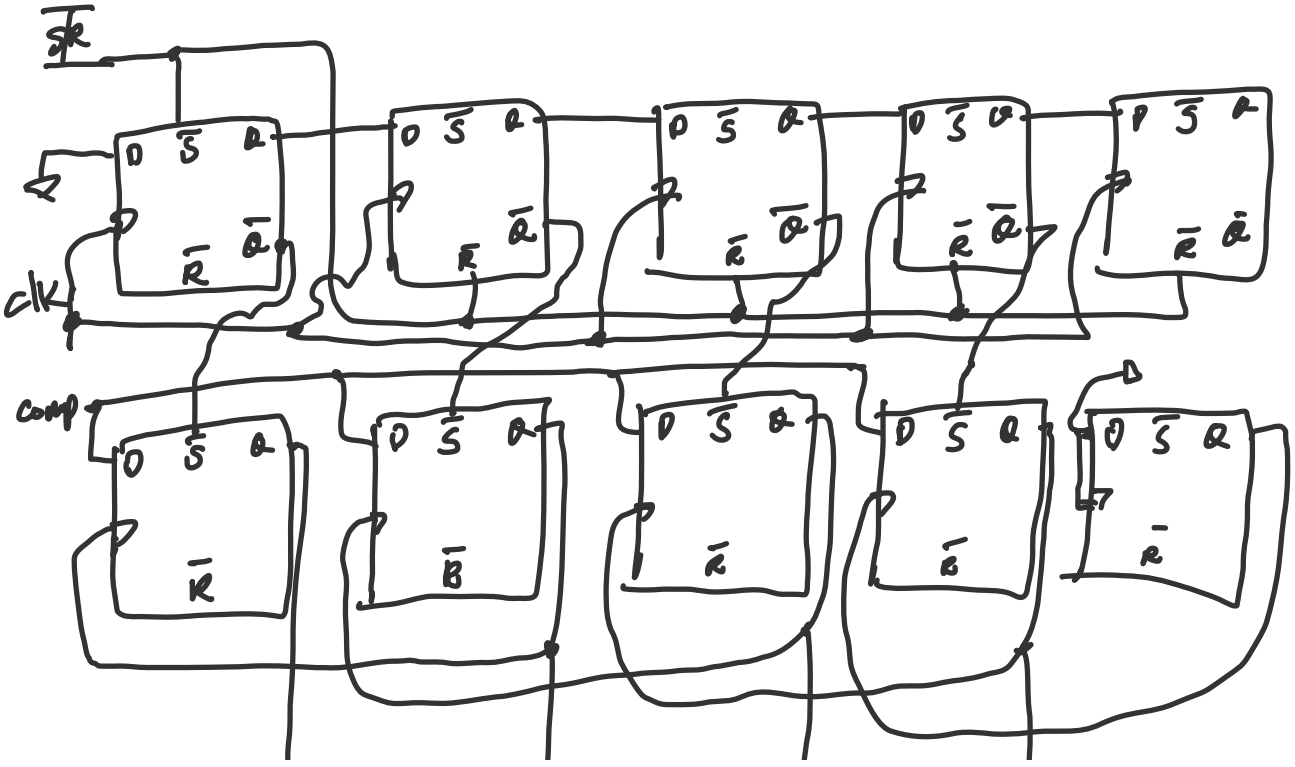
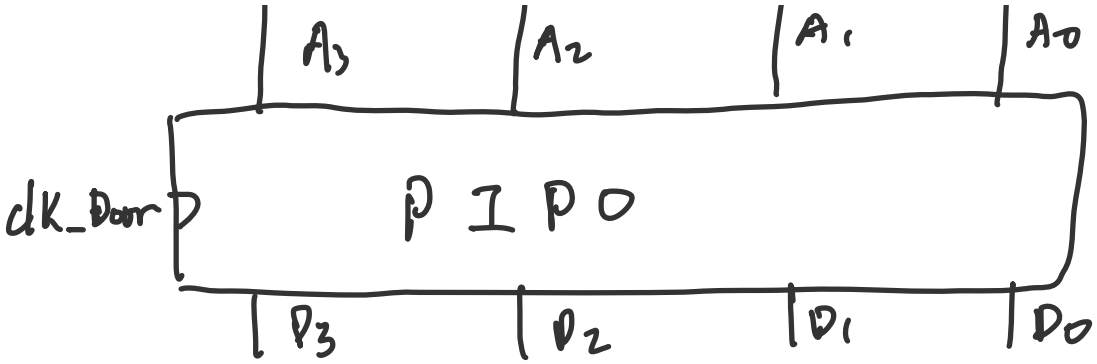
SAR ADC 2025

Sunday, March 9, 2025 11:06 AM

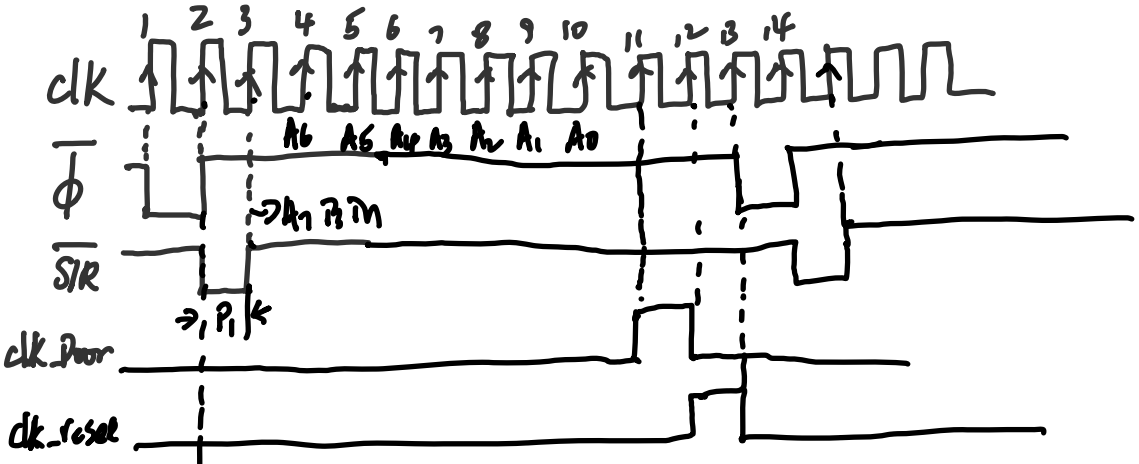


- ✓ $\bar{\phi}=1$, reset, Hold
- ✓ $\bar{\phi}=0$, sample/track
- ✓ $\phi=1$, (A) shorted to (B), Vdd across C_3 is applied to V_{SG} of M_8. M_8 is on
- ✓ S got pushed into C_3, $V_{C_3}=V_{SG_{M_8}}=V_{dd}+V_S-V_S=V_{dd}$ constant V_{SG} for M_8
- ✓ M_8 passes the entire $V_{dd}+V_S$ to (C)
- ✓ when V_S exceeds $V_{dd}-V_{thN}$, M_5 is off. Adding M_{13} there can keep V_G of M_8 to be V_S in this situation.





Final Digital Output



- $\overline{\phi}$ back to 1, S/H starts holding, $\overline{S/R}$ resets, SAR outputs 1000…
- P_1 gives ADC the time to output A_7, rising edge 3 latches A_7 in by sending a '1' to the first DFF's clk.