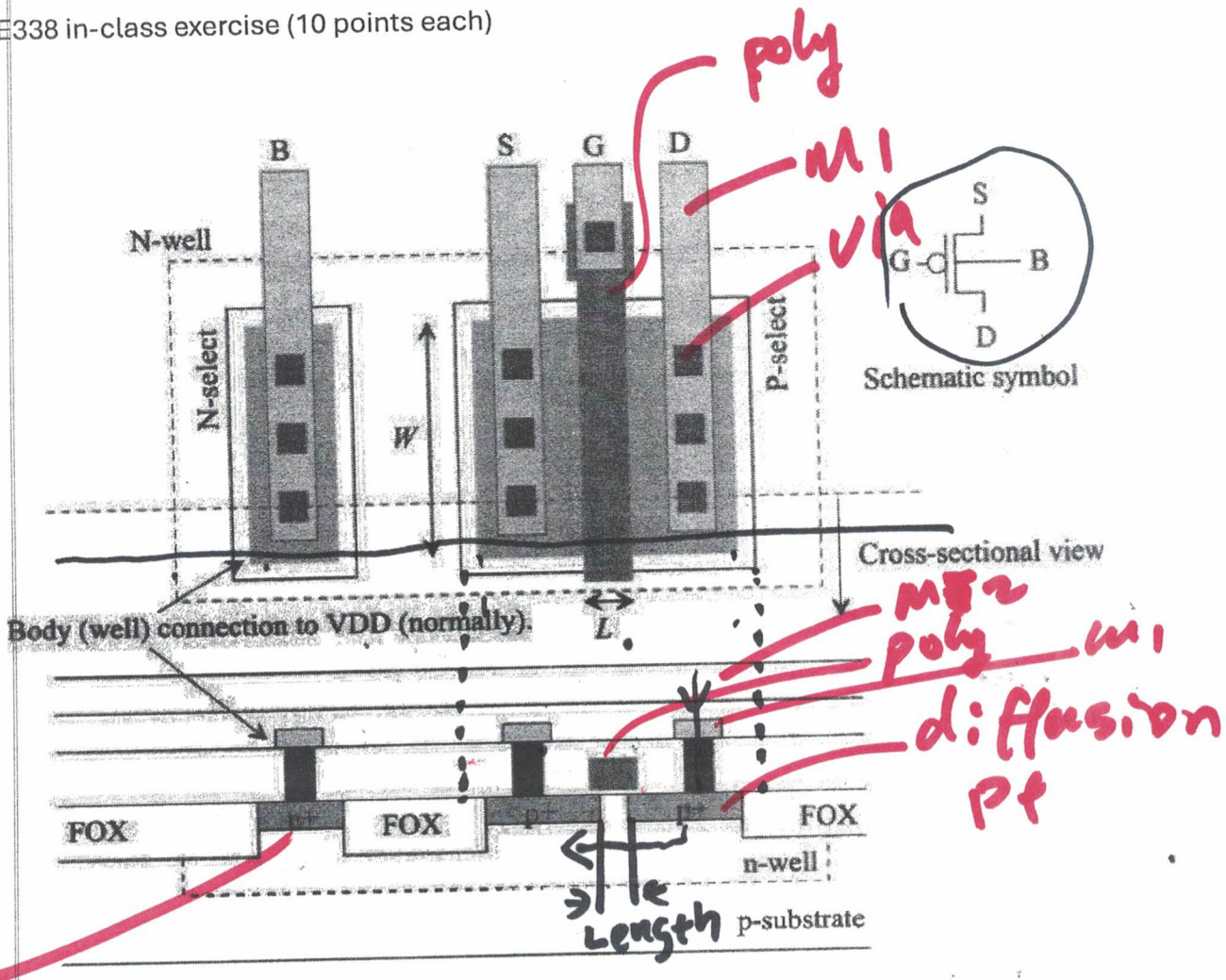
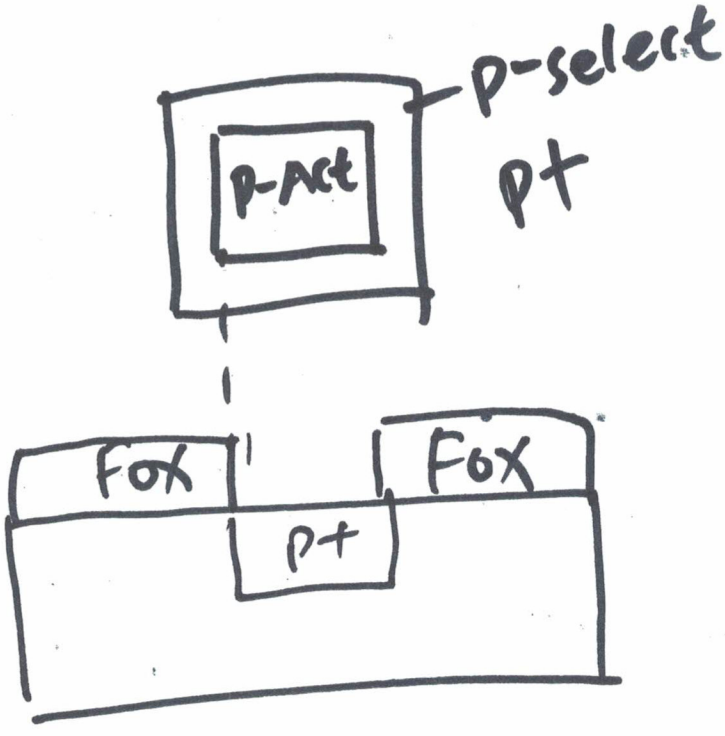


Figure 4.13 Layout and cross-sectional views of an PMOS device.



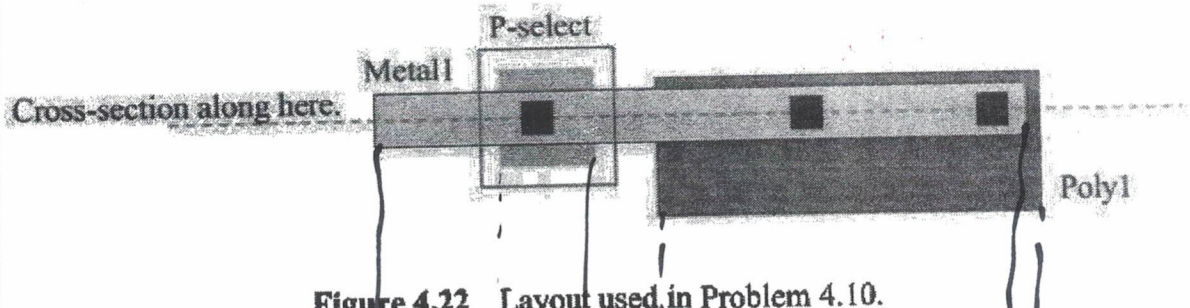
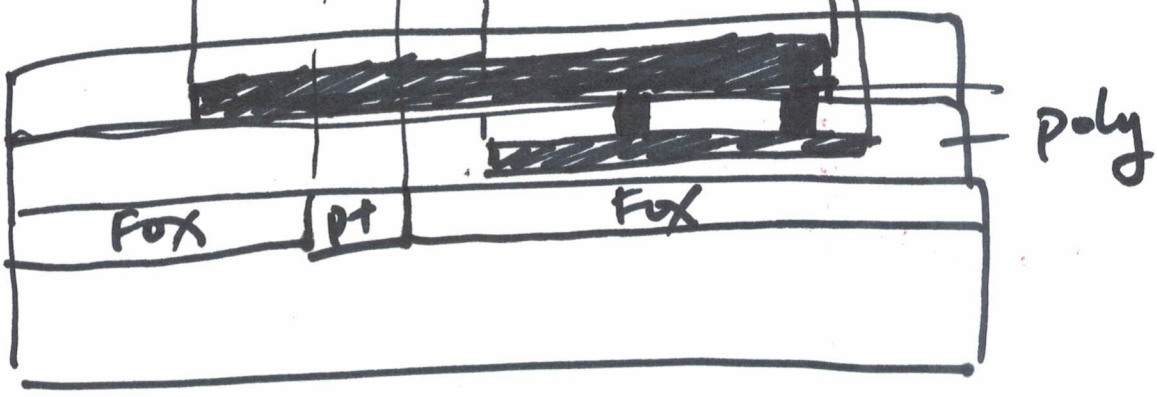


Figure 4.22 Layout used in Problem 4.10.



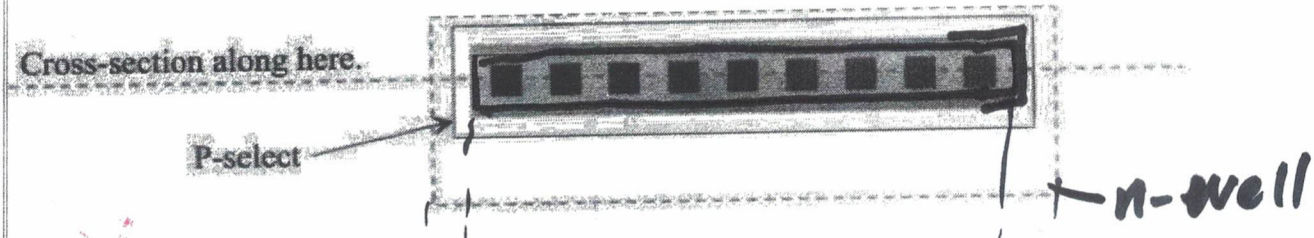
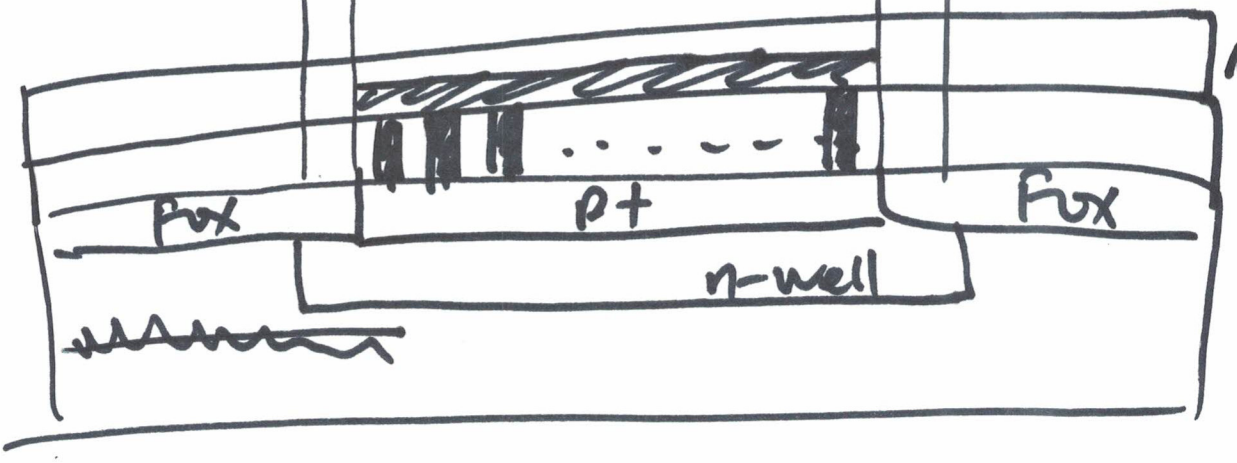
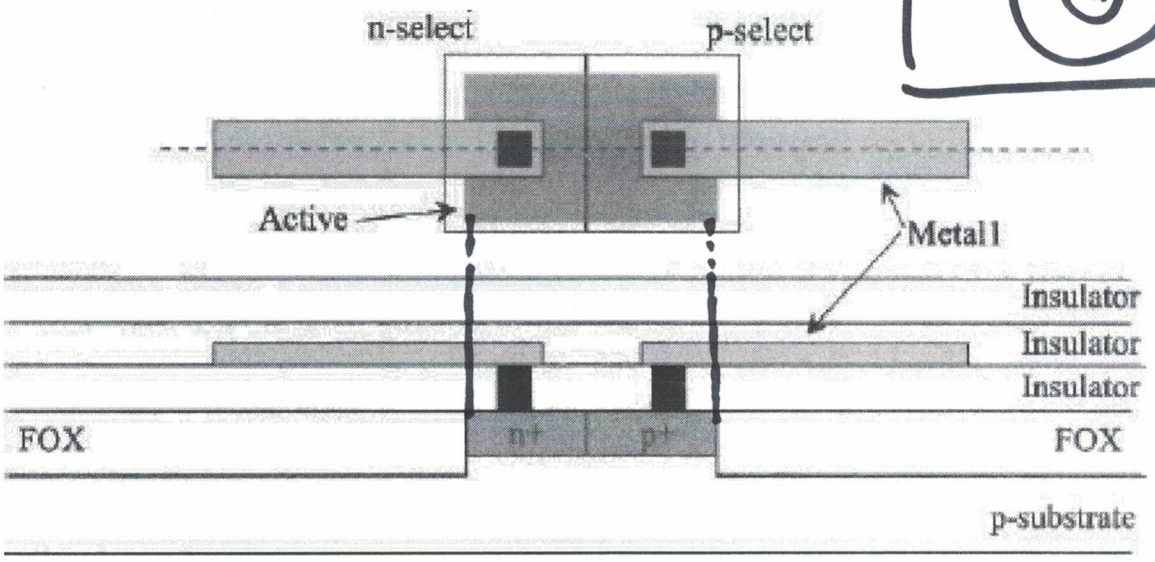
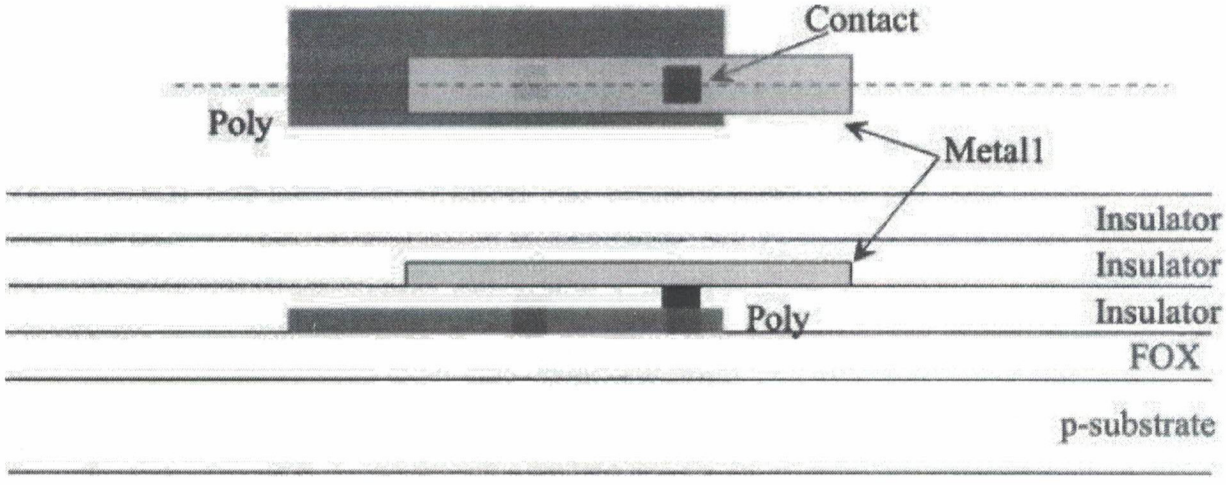


Figure 4.23 Layout used in Problem 4.11.

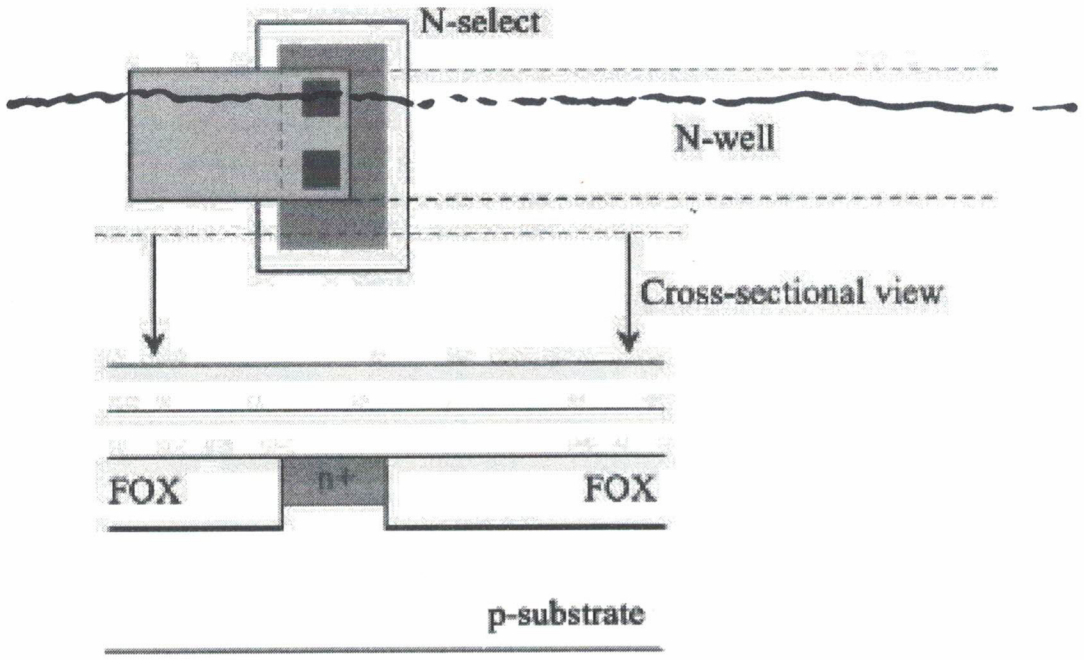


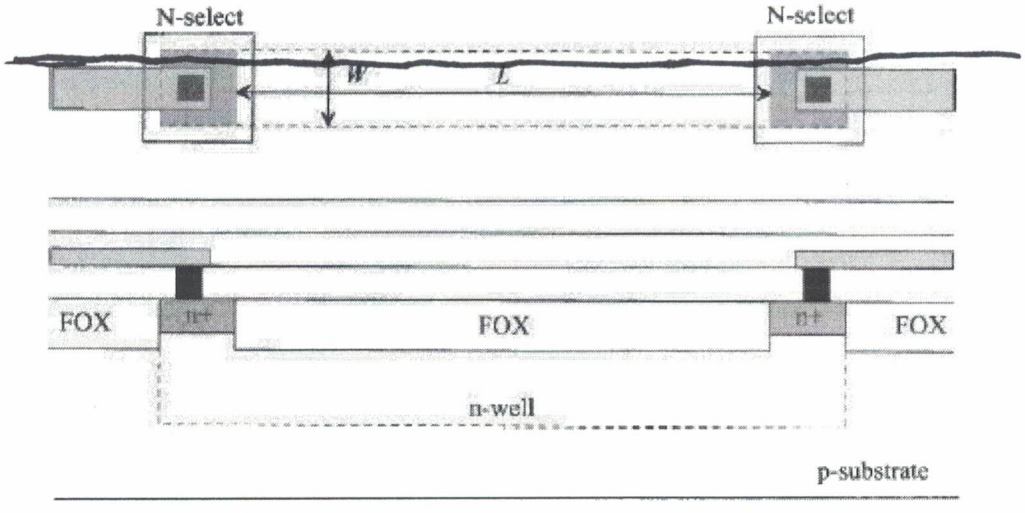
CE338 in-class exercise (10 points each)

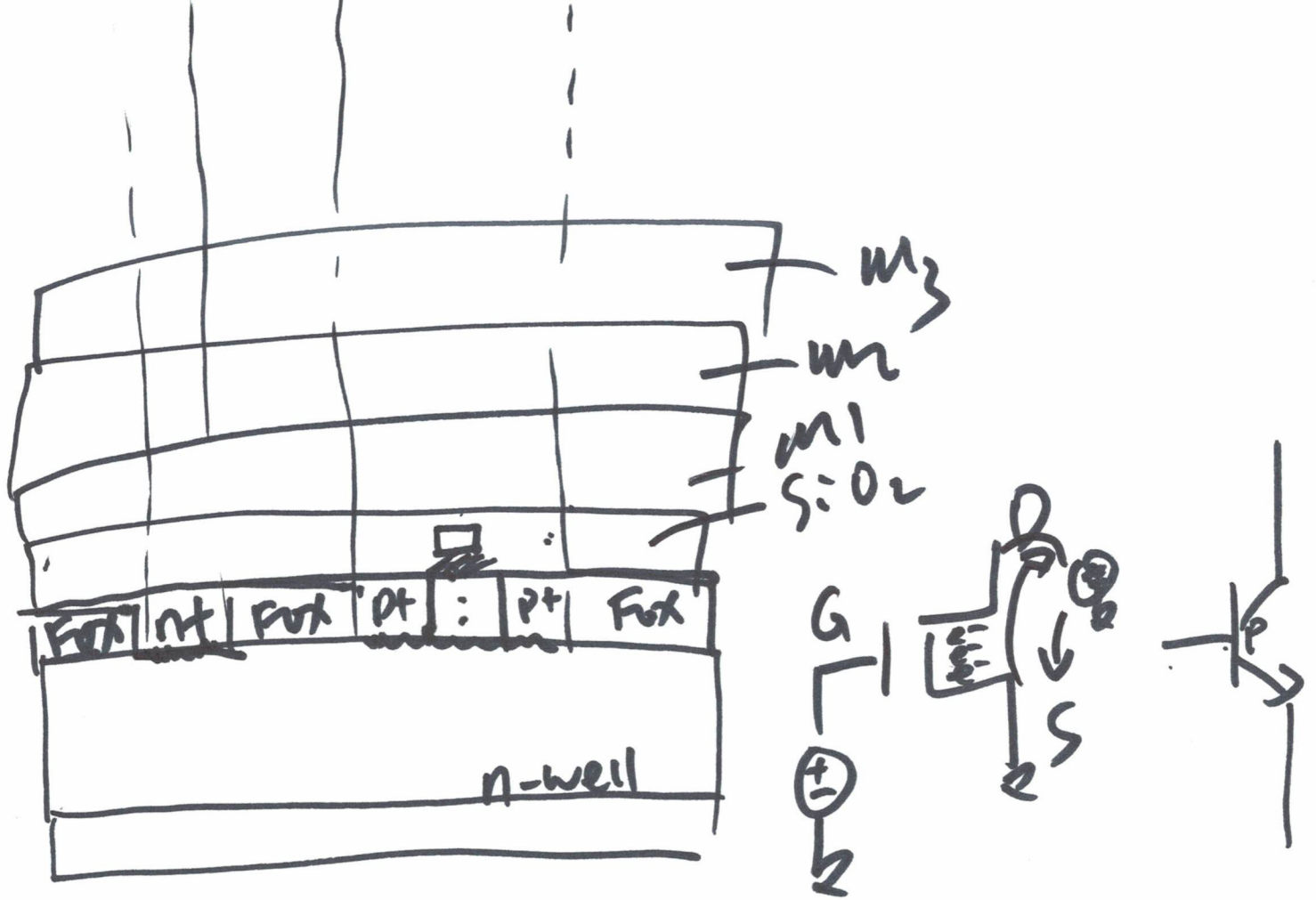




CE338 in-class exercise (10 points each)






m3
m2
m1
SiO2
Fox
n+
Fox
p+
:
p+
Fox
n-well
G
S