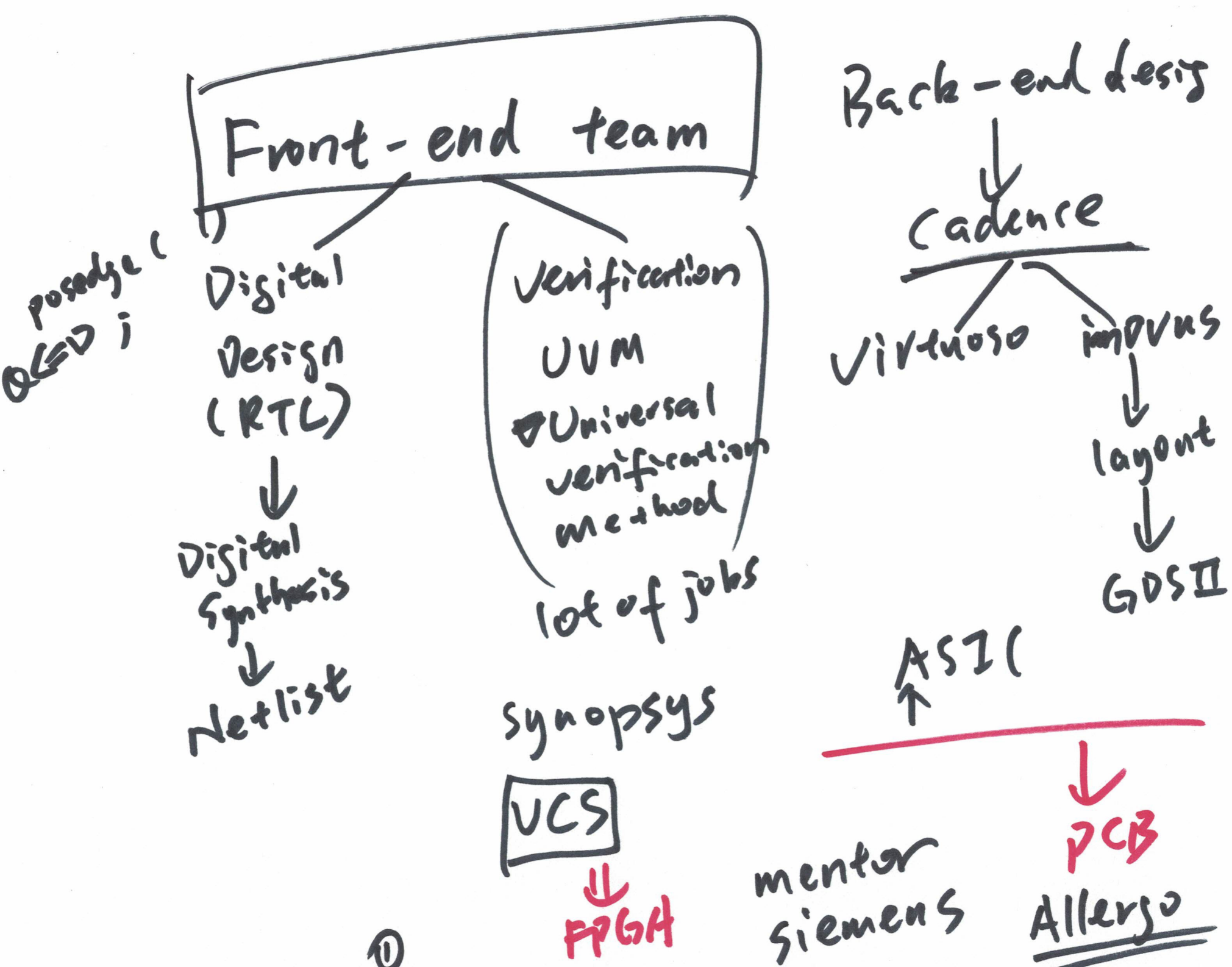
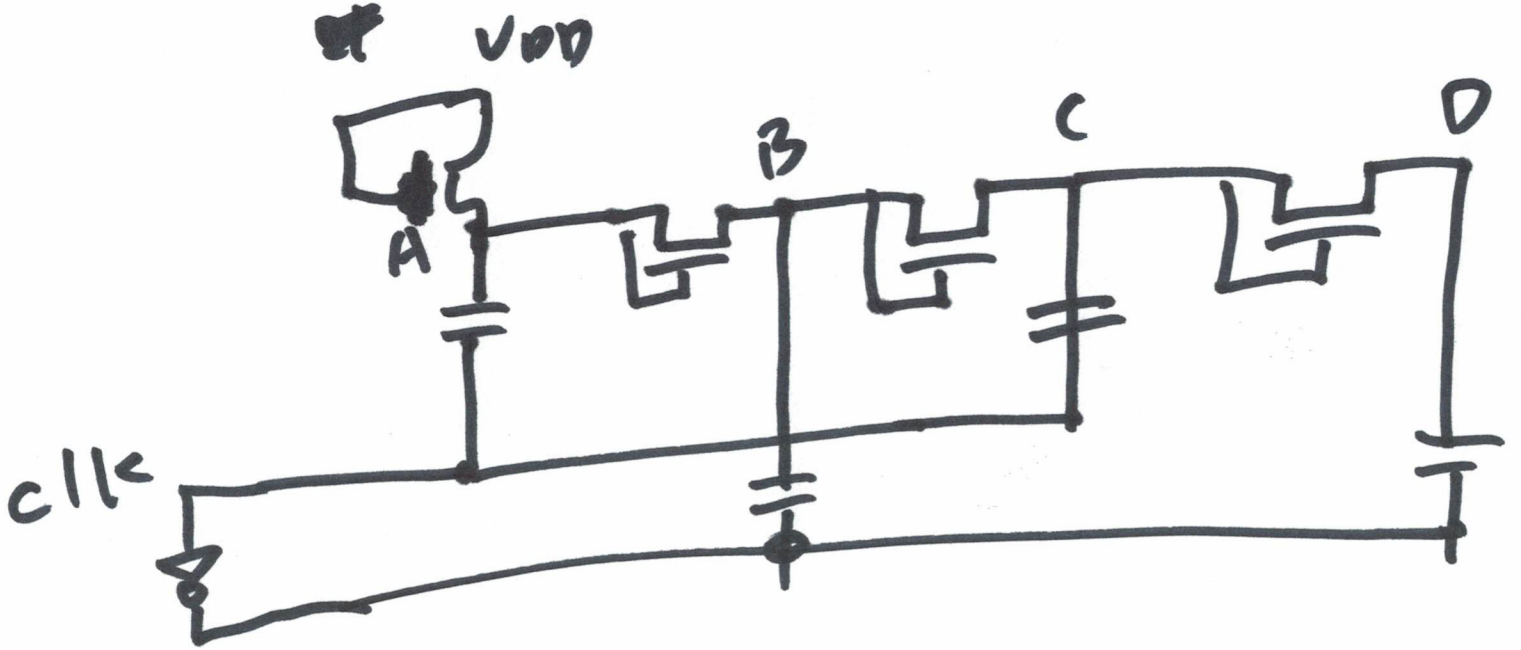

Front-end team
Digital Design (RTL)
Digital Synthesis
Netlist
Verification
UVM
Universal verification method
lot of jobs
synopsys
UCS
FPGA
Back-end desig
Cadence
Virtuoso
innovus
layout
GDSII
ASIC
PCB
mentor siemens
Allergo



A

$V_{DD}-V_{THN}$ (pulls)

$2V_{DD}-V_{THN}$ (pushes)

B

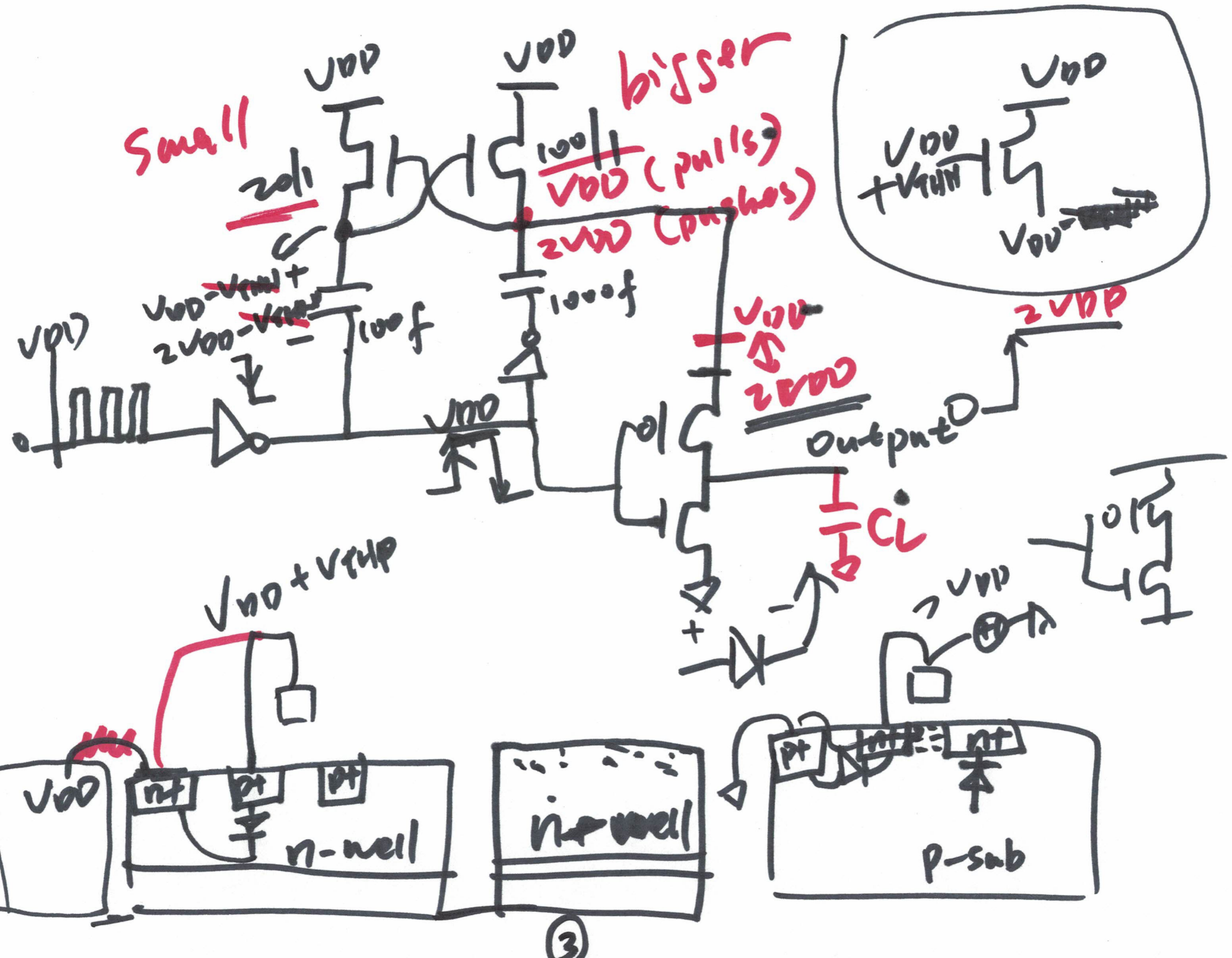
$3V_{DD}-2V_{THN}$ (pushes)

$2V_{DD}-2V_{THN}$ (pulls)

C

$3V_{DD}-3V_{THN}$ (pulls)

$4V_{DD}-3V_{THN}$ (pushes)


Small
VDD
VDD
bigger
100f
VDD (pulls)
2VDD (pushes)
VDD
+VtHN
VDD
2VDD
100f
100f
VDD-
2VDD
2VDD
output
Ci
VDD+VtHP
VDD
n+
p+
p+
n-well
n-well
p+
n+
p-sub
3