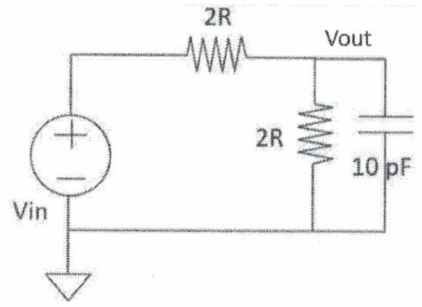
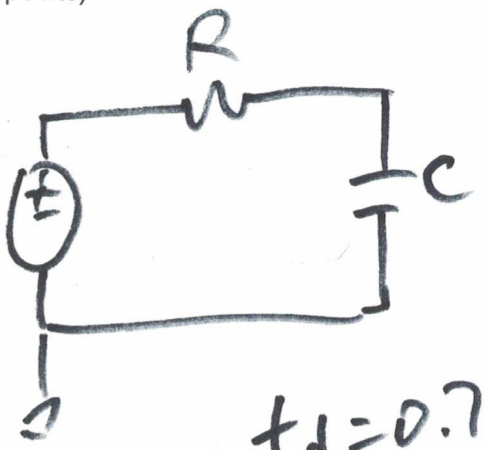
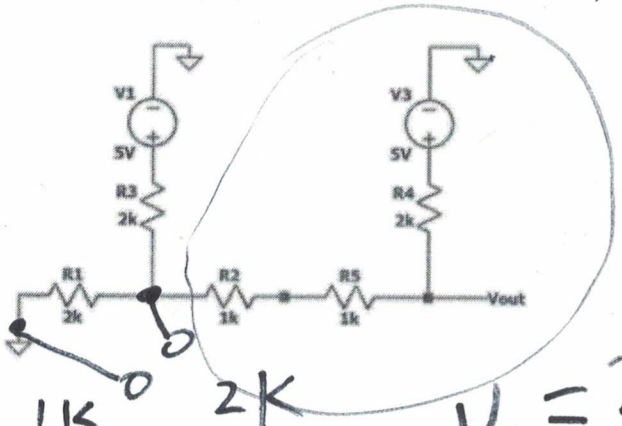
1. R = 10k, determine time delay at Vout. (15 points)

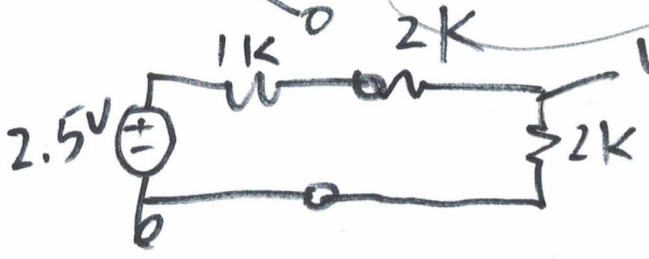




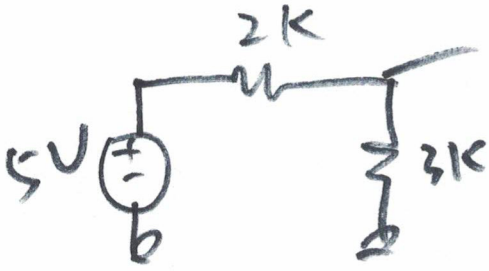
$t_d = 0.7RC$

2. Use Thevenin's equivalent theory and superposition to solve for Vout in the following circuit (show the process/equivalent circuits for full credit). (15 points)





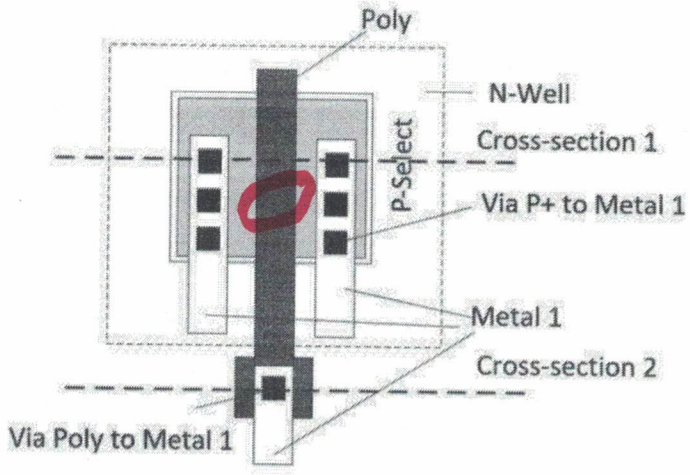
$V_1 = 2.5V \cdot \frac{2K}{5K} = 1V$

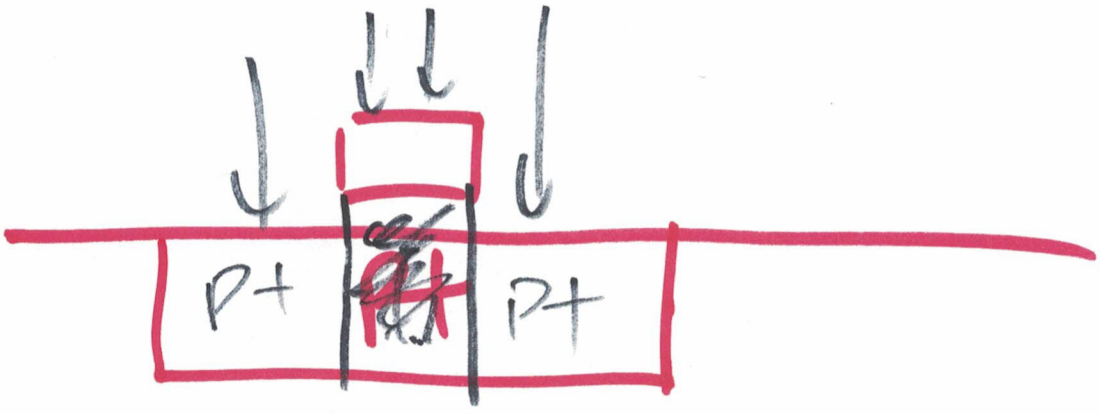


$V_2 = 5V \cdot \frac{3K}{5K} = 3V$

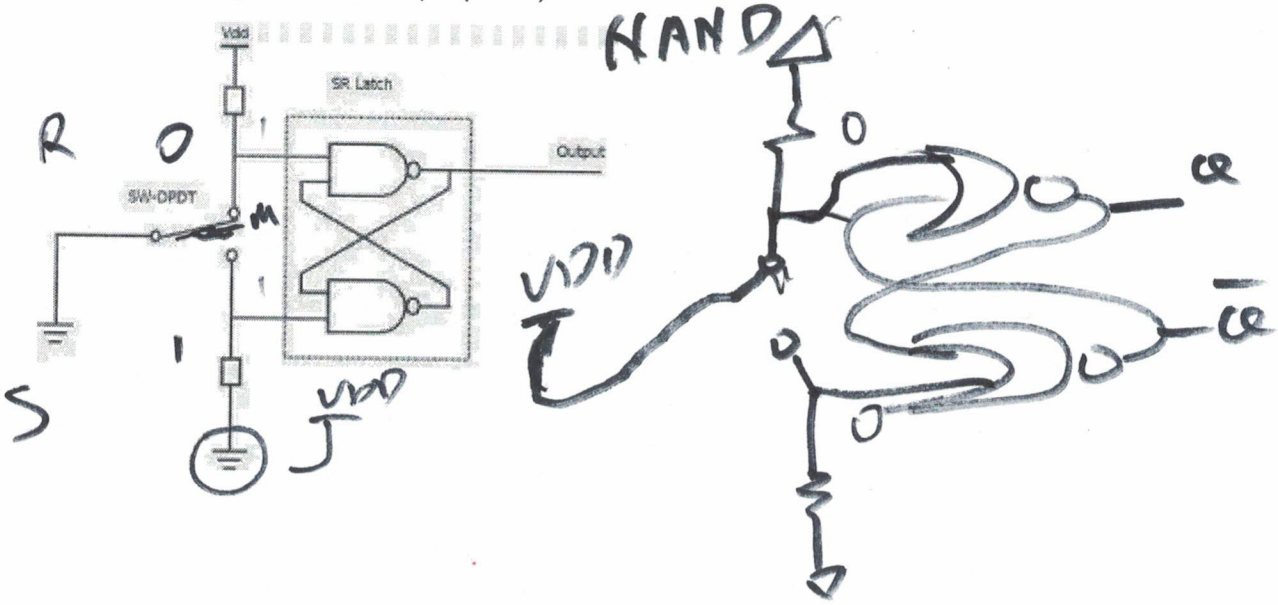
$V_{out} = V_1 + V_2 = 4V$

3. The following figure shows the top-view of a layout. Draw the cross-sectional views (cross-section 1 and cross-section 2 of the locations indicated by the dashed lines. (15 points)

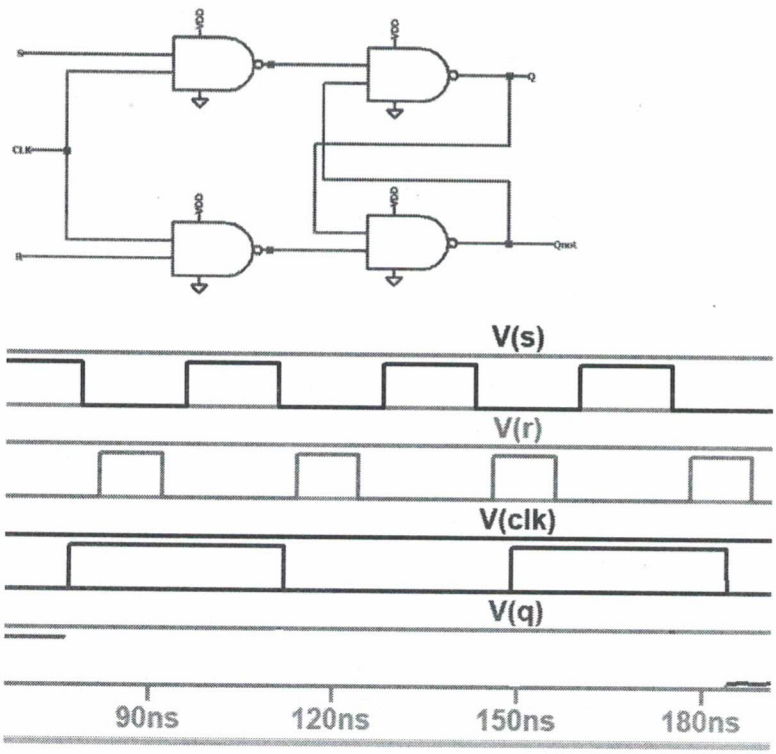




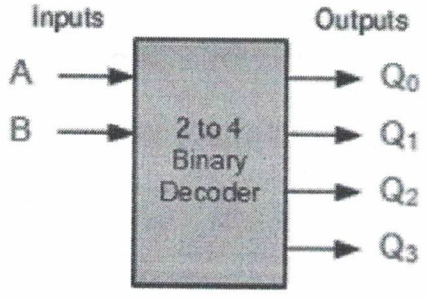
4. A debounce circuit is an electronic circuit that eliminates false switching signals caused by the mechanical bouncing of switch contacts, providing a clean, single output signal to a digital circuit. Would the following circuit serve as a debounce circuit? Why or why not? If it wouldn't, how to fix it? What are the typical resister values of the two resistors? Design a debounce circuit that uses NOR gates instead. (15 points)



5. Complete the following waveforms of the DFF output V(q). (15 points)



6. Find the AOI schematic and the stick diagram of output Q3 for the following decoder. Note that the signal input is A and B, output is Q3. If A_not or B_not signals are needed, you need inverters to invert A and B. The stick diagram should include all circuits between the power and GND rails. Gates should be labeled and aligned. (25 points)



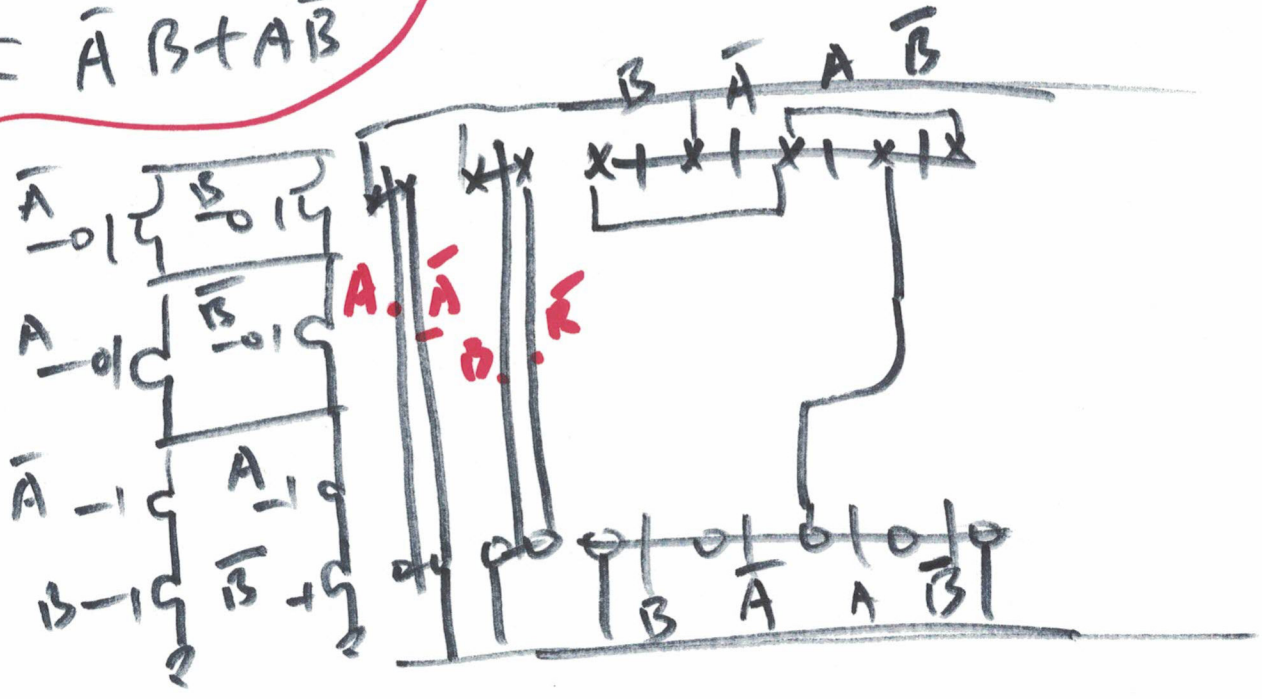
Truth Table

A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$Q_3 = \bar{A}\bar{B} + AB$

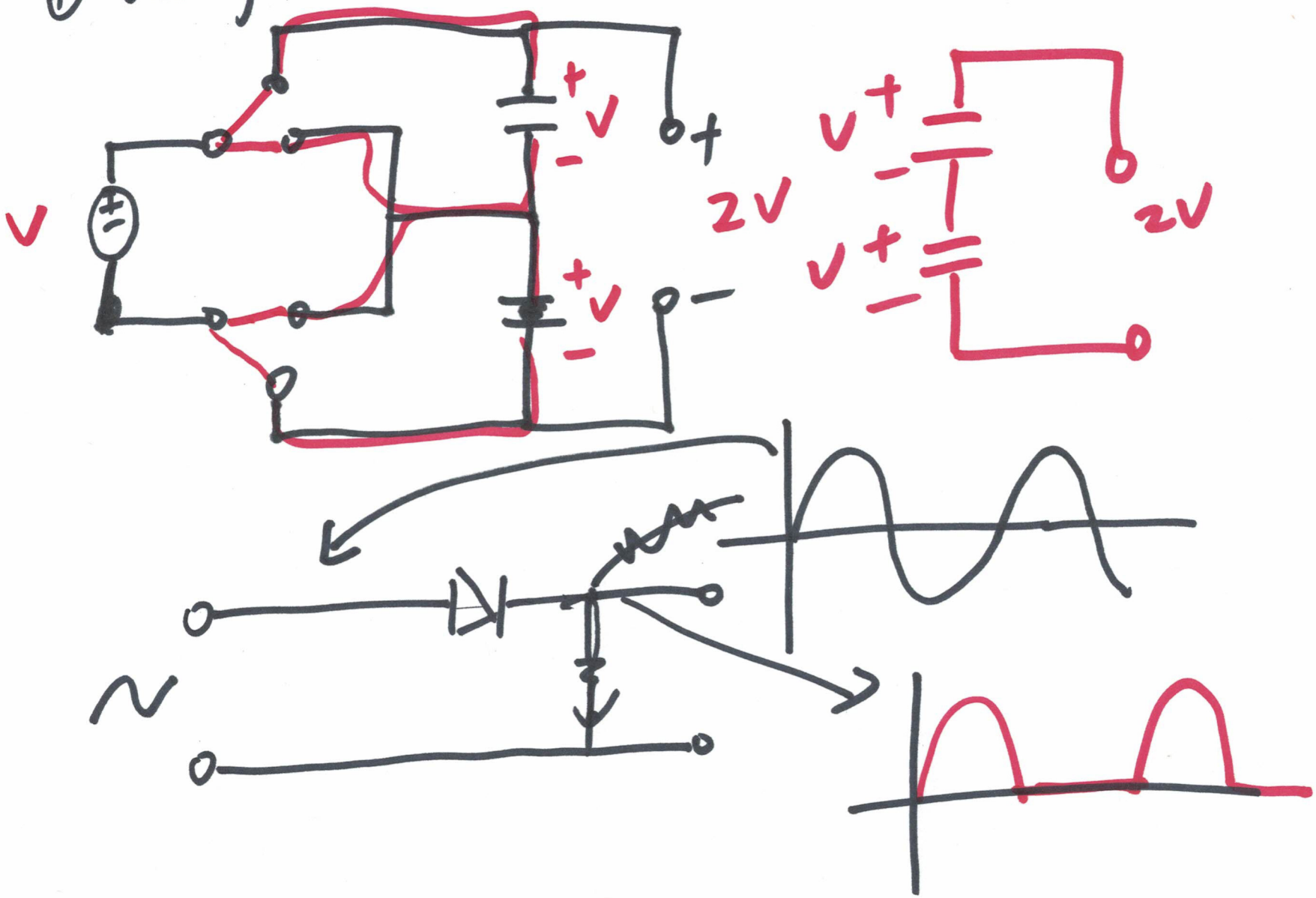
XNOR = $\overline{\text{XOR}}$

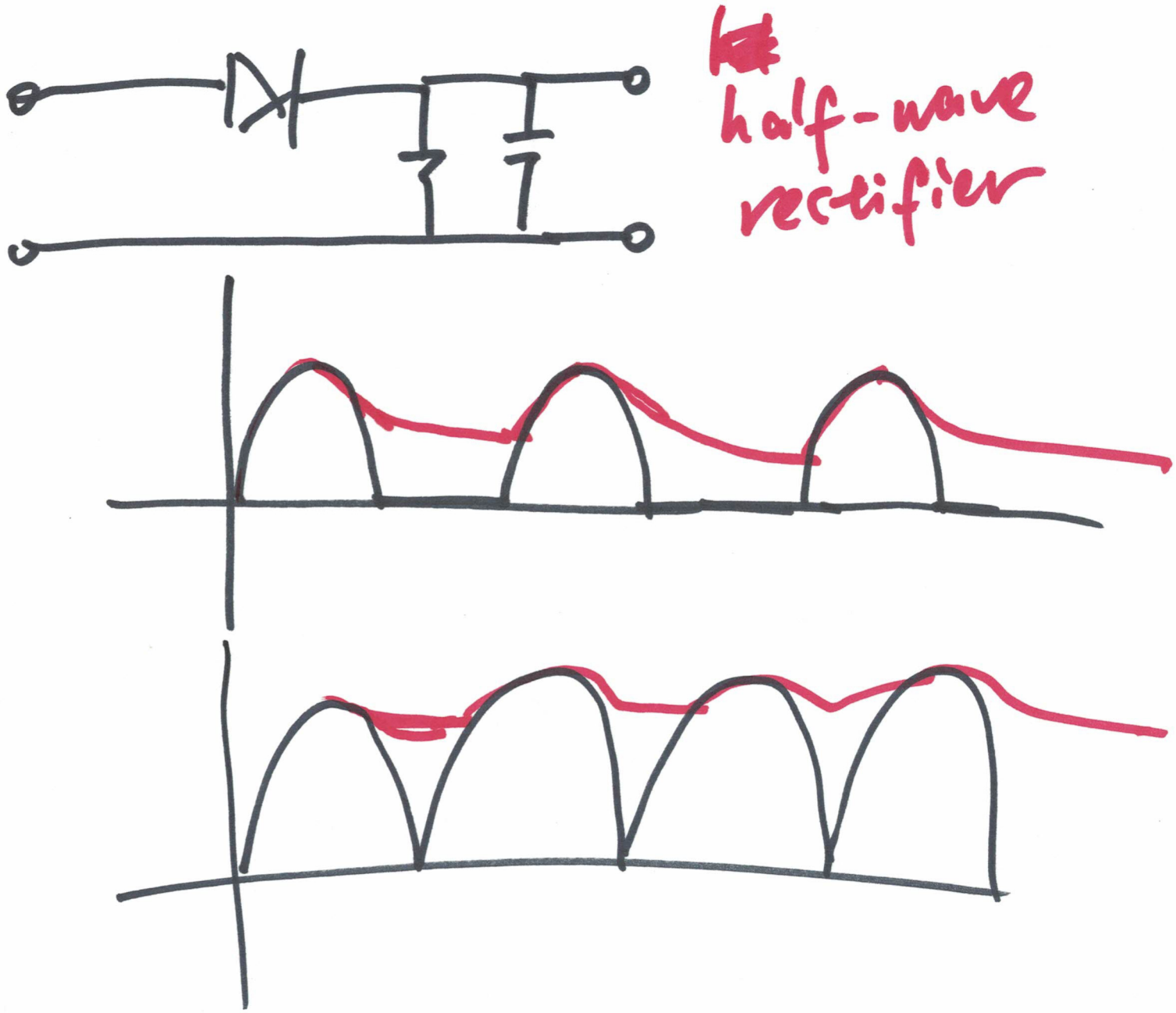
$= \bar{A}B + A\bar{B}$

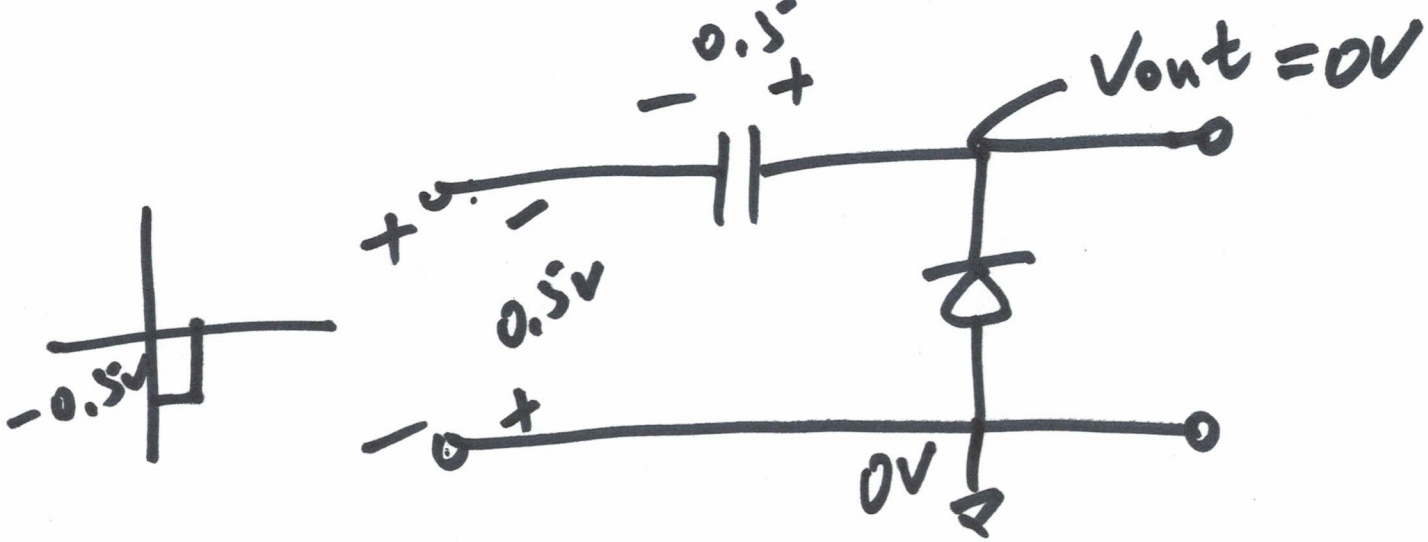


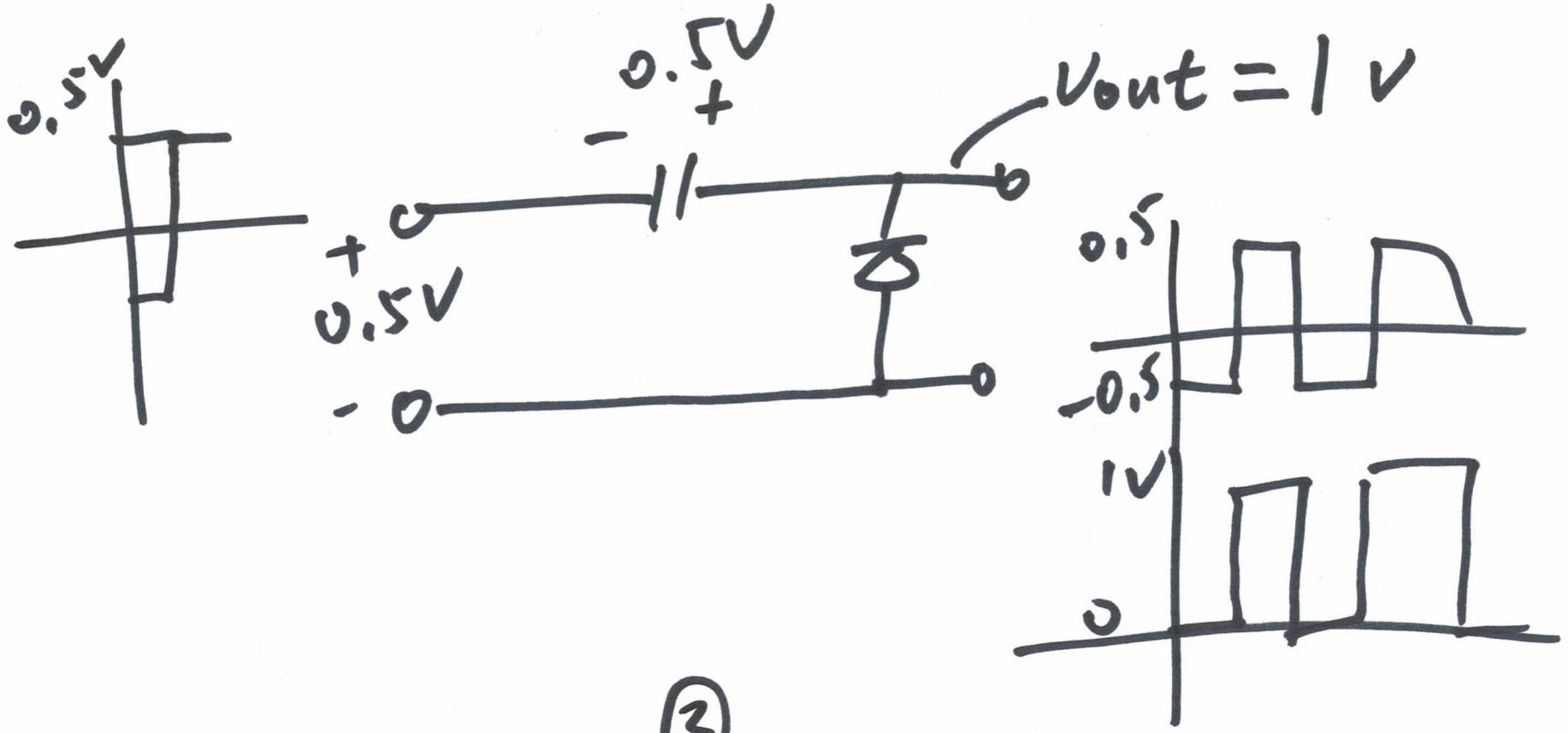
The Charge Pump

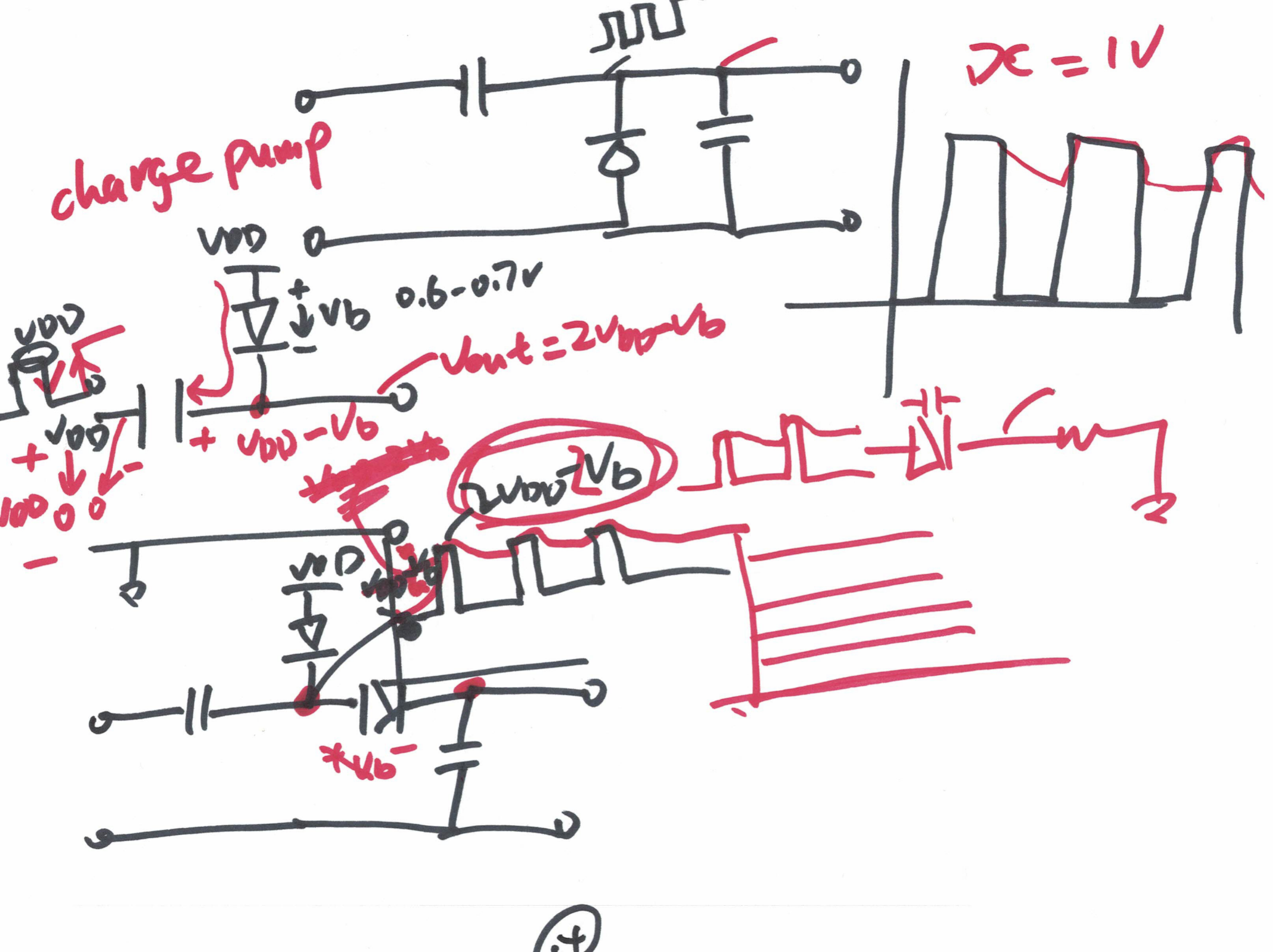
① Voltage Doubler

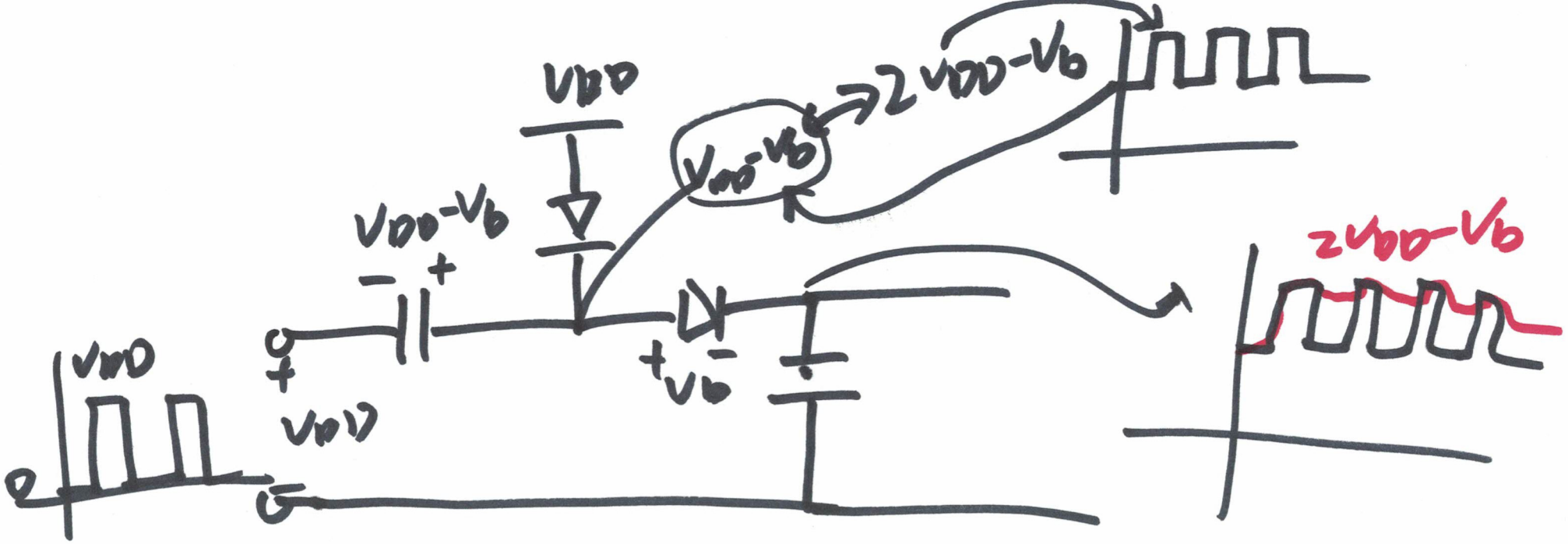



half-wave
rectifier


0.5
Vout = 0V
0.5V
-0.5V
0V


0.5V
0.5V
Vout = 1 V
0.5V
0.5
-0.5
1V
0


charge pump
VDD
Vb
0.6-0.7V
Vout = 2VDD-Vb
VDD - Vb
2VDD-2Vb
*Vb
x = 1V


VDD
VDD-Vb
VDD-Vb
2VDD-Vb
VDD
VDD
+Vb
2VDD-Vb