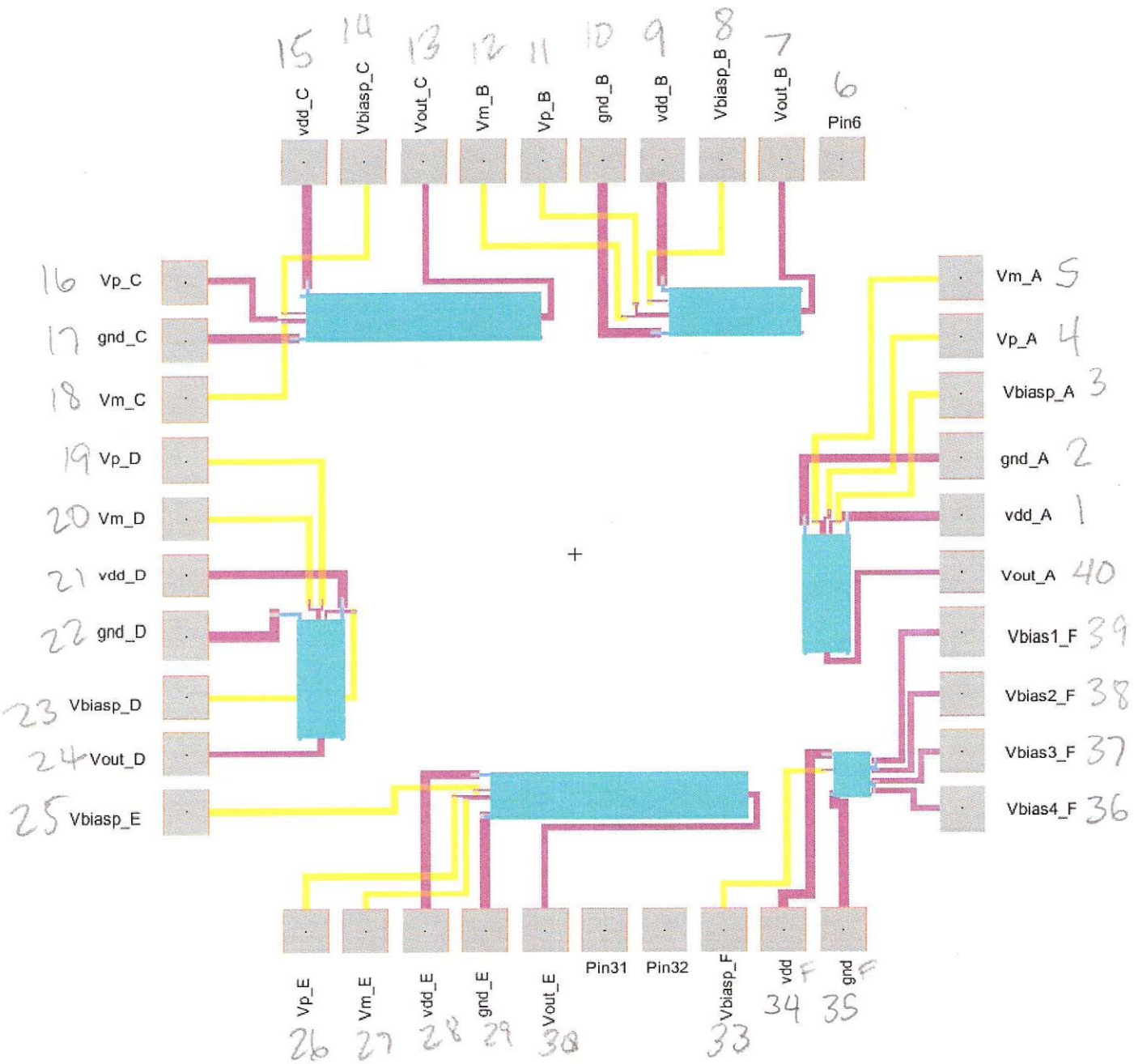
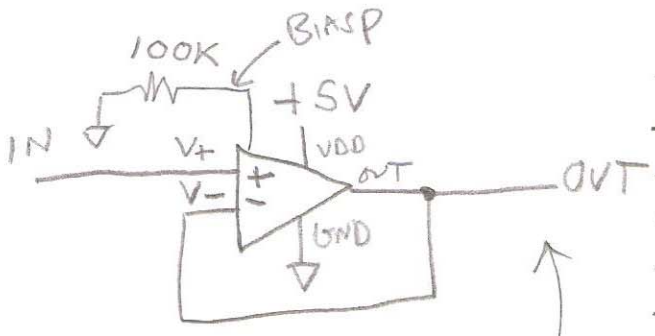




Design	V+	V-	OUT	VDD	GND	BIASP
A	4	5	40	1	2	3
B	11	12	7	9	10	8
C	16	18	13	15	17	14
D	19	20	24	21	22	23
E	26	27	30	28	29	25

+5V

.01μF

decoupling

No resistive load

C_L < 30 pF

F is bias circuit

33 → 100K

34 → VDD 35 → GND

36 → 39 → bias voltages

1)

Image of chip with the cover removed. DO NOT REMOVE COVER!!!

Showing pin numbers.

PIN 1

PIN 40

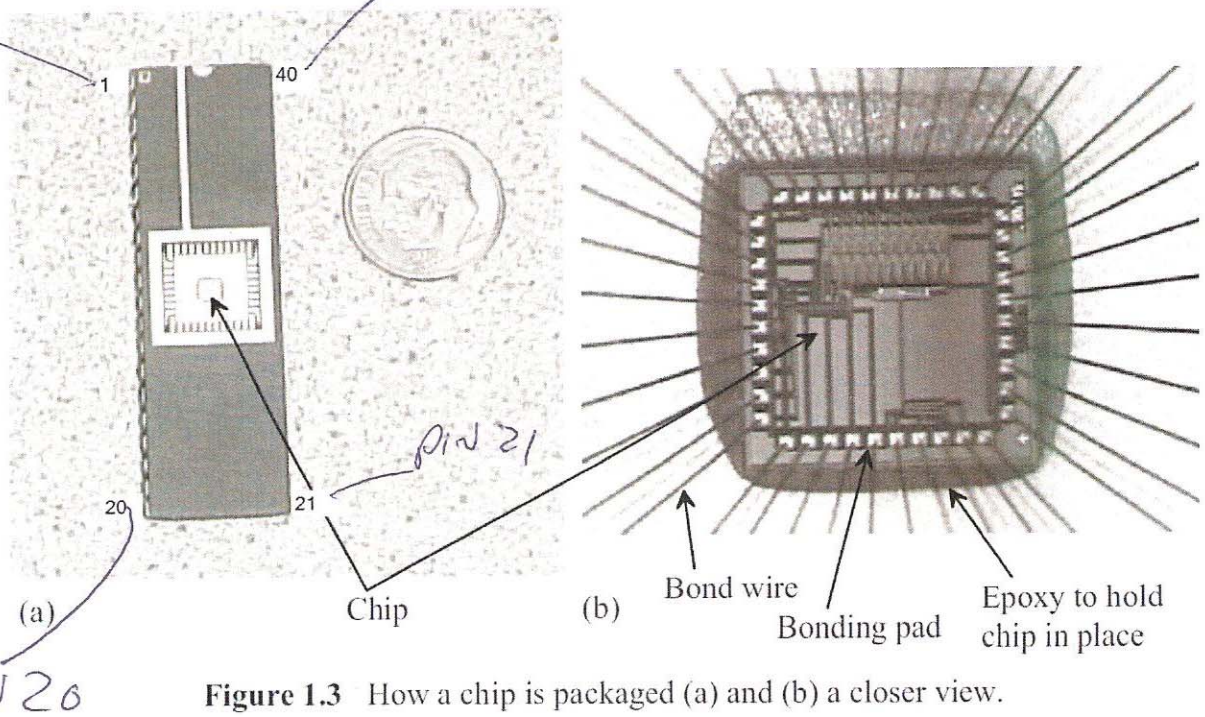
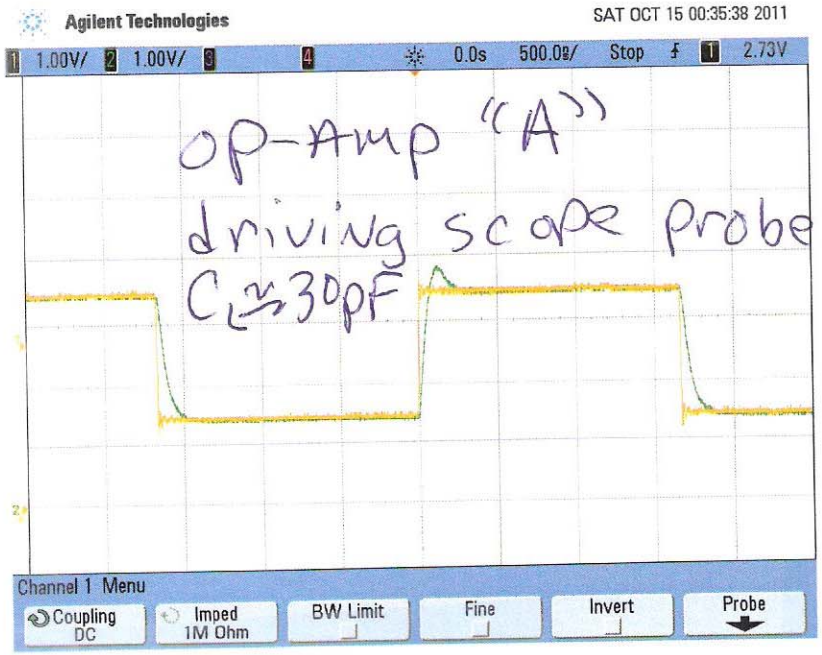


Figure 1.3 How a chip is packaged (a) and (b) a closer view.



INPUT offset =

2.5 V

Swing 2 V

INPUT → 1.5 V

↓

3.5 V

2)