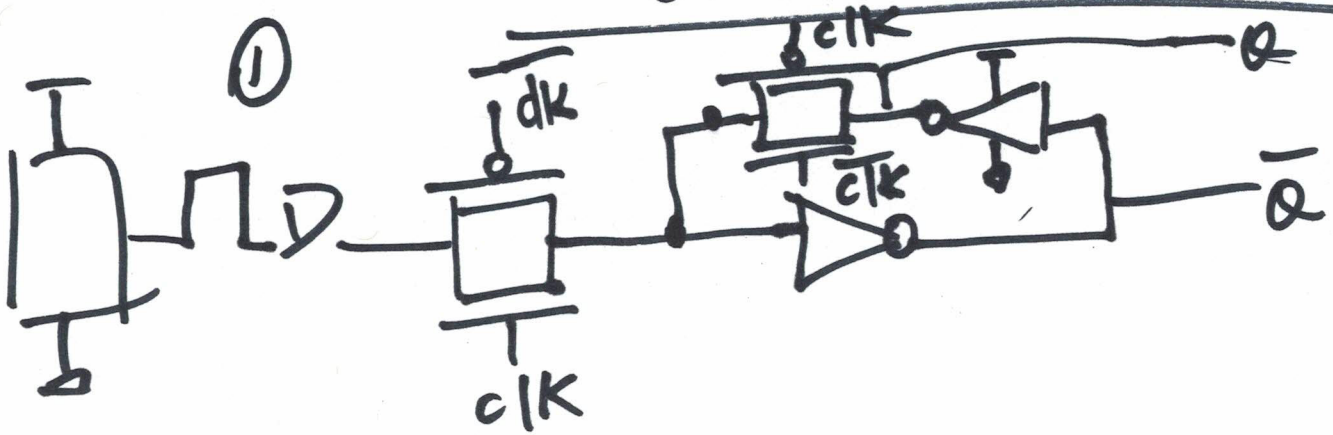
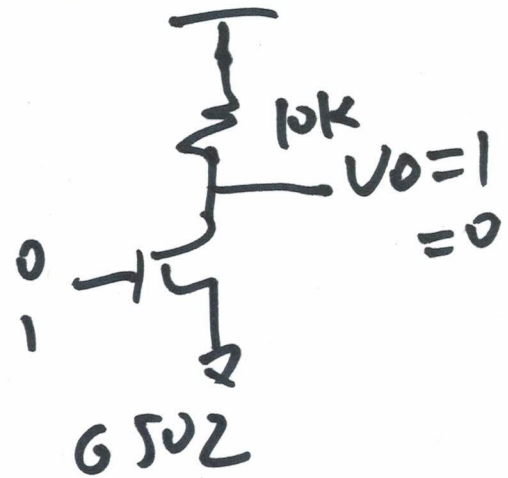
clocked Circuit

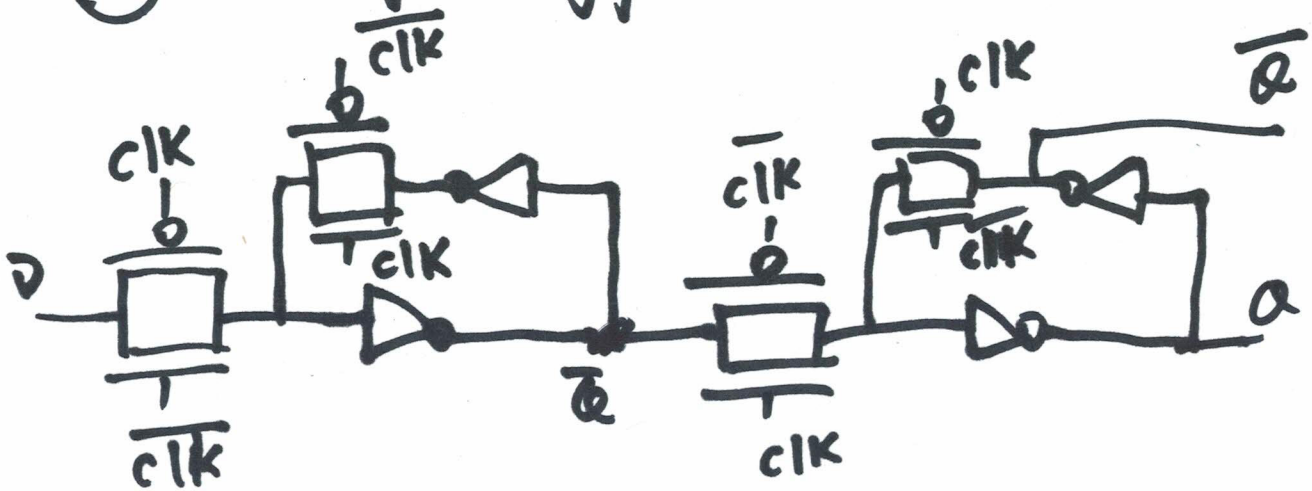
① 

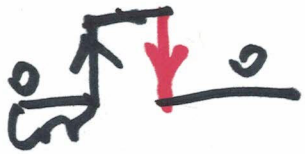
Transmission Gate (TG)

Pass Gate (PG)

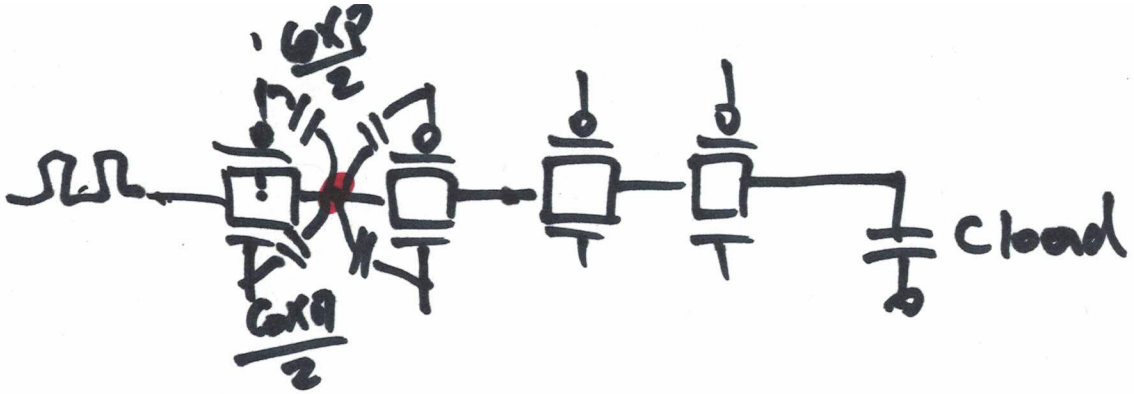


② An Edge Triggered DFF

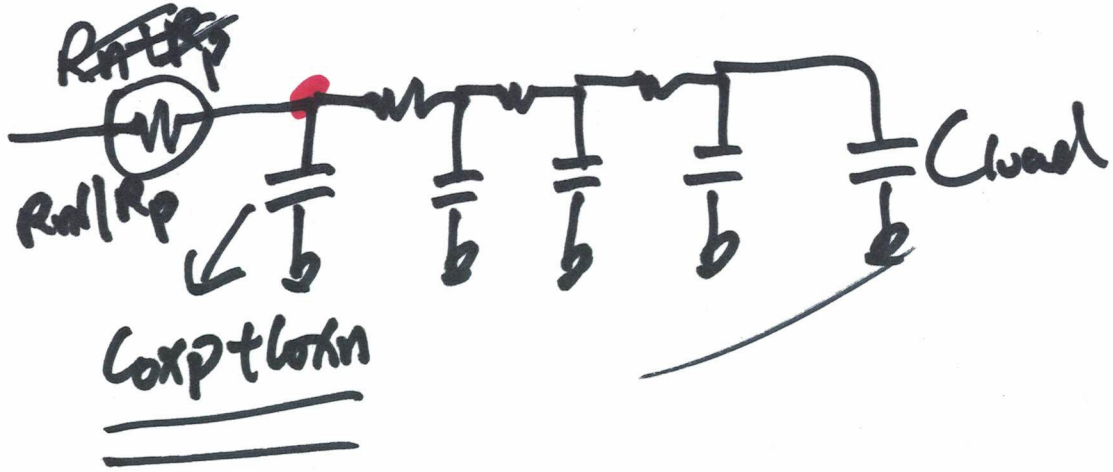


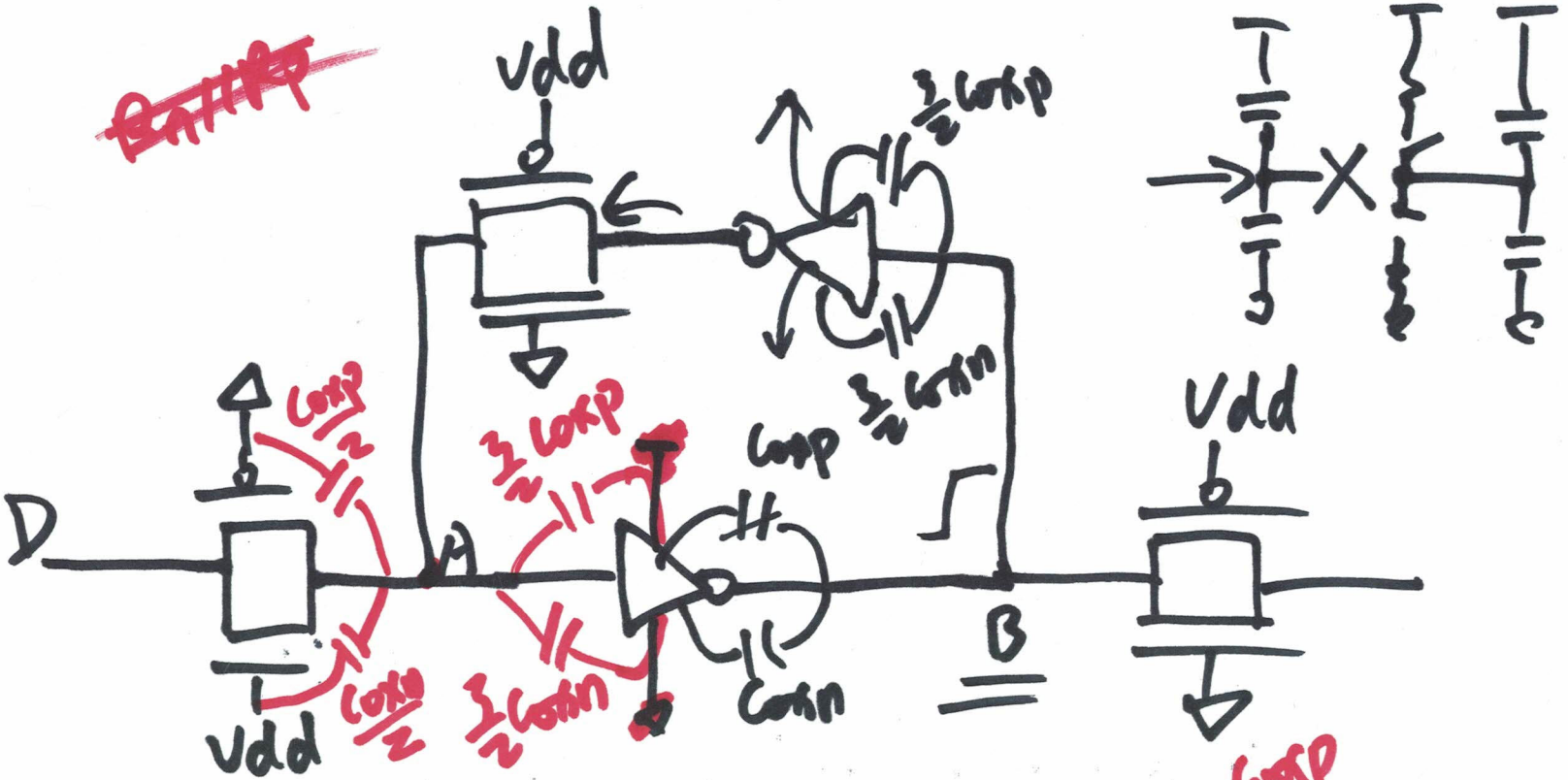


③



RC digital model for TGs.





NMOS: $R_n = 3.4K$, $C_{oxn} = 0.625fF$.

PMOS: $R_p = 3.4K$, $C_{oxp} = 1.25fF$

td: D → A

A → B

D - B

$$C_A = 2(C_{oxp} + C_{oxn})$$

$$C_B = \frac{5}{2}(C_{oxp} + C_{oxn})$$

Delay from D to A:

$$t_{pHL_A} = t_{pLH_A} = 0.7 \cdot (R_n \| R_p) \cdot C_A$$

(3)

Delay from A to B:

$$t_{PLH_B} = 0.7 \cdot R_p \cdot C_B$$

$$t_{PHL_B} = 0.7\, R_n\, C_B$$

The propagation delay from D to B:

$$t_{PLH} = t_{PLH_A} + t_{PLH_B}$$

$$t_{PHL} = t_{PHL_A} + t_{PHL_B}$$

SRAM DRAM SDRAM ROM ~~FLS~~ FLASH

EROM EEPROM EEPROM Electrically

Erasable programmable

E^2PROM

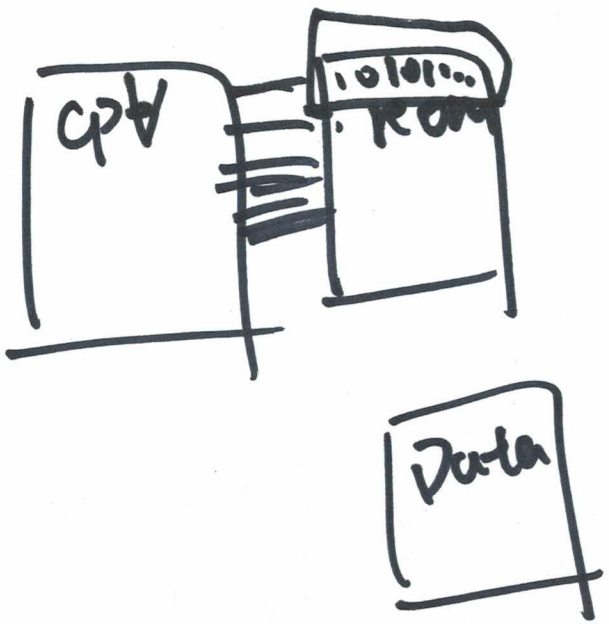
RAM: Random Access Memory volatile? Yes.

SRAM: static RAM

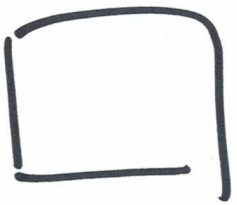
DRAM: Dynamic RAM

SDRAM: Synchronous DRAM

ROM: Read Only Memory



{ Micron → Boise, ID
  Samsung → S. Korea



DDR (SDRAM)
↳ Double Data Rate

DDR4.
DDR5 → 2020