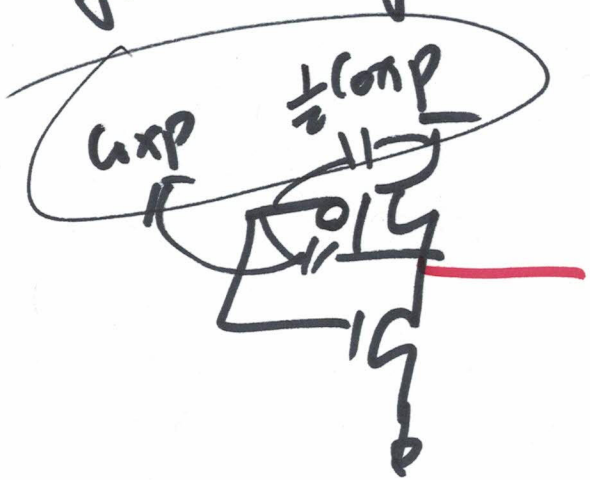
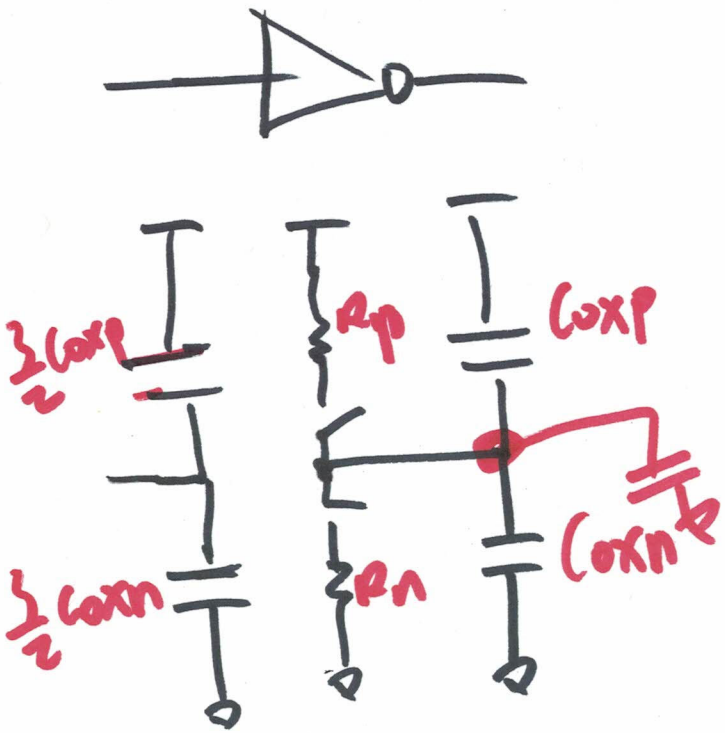
Models for Digital Design





△ Estimate the intrinsic propagation delay of the following inverter.

P320

NMOS: 10/1, 0.5μm/50nm.

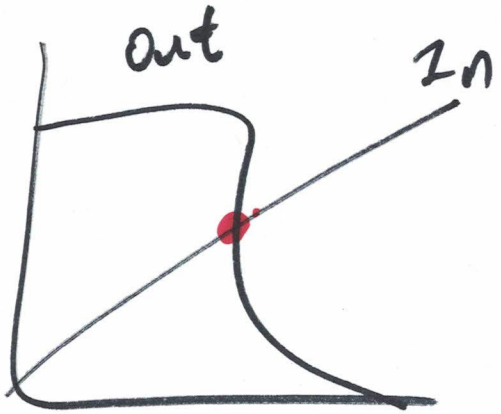
$R_n = 3.4K$ $C_{oxn} = 0.625fF$

PMOS: 20/1, 1μm/50nm, $R_p =$ 3.4K,

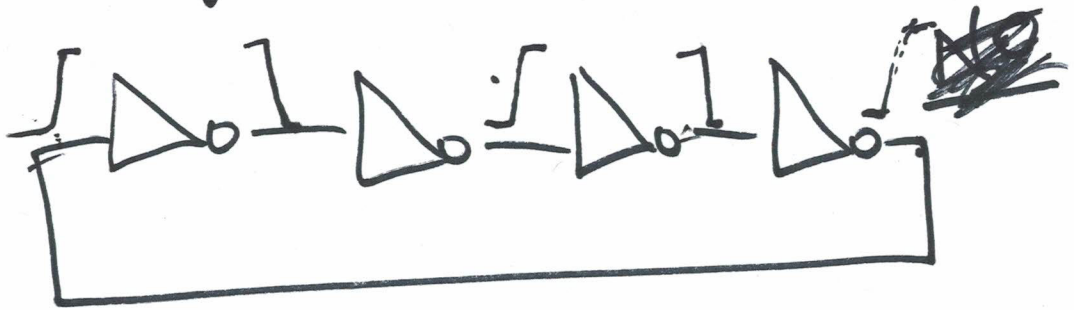
$C_{oxp} = 1.25fF$.

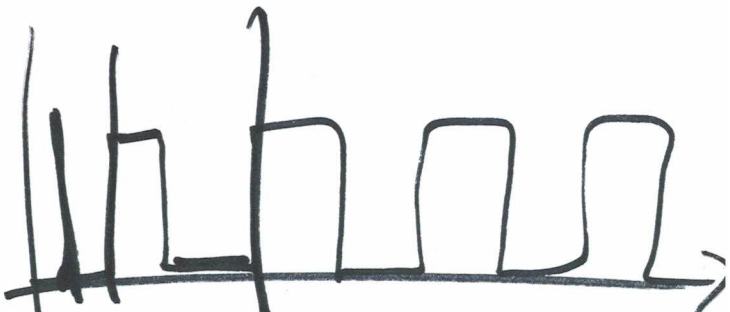
$t_{pLH} = 0.7 \cdot R_p C_{tot} = 0.7 \cdot 3.4K \cdot (C_{oxp} + C_{load})$

$t_{pHL} = 0.7 \cdot R_n \cdot C_{tot} = \ldots\ldots$

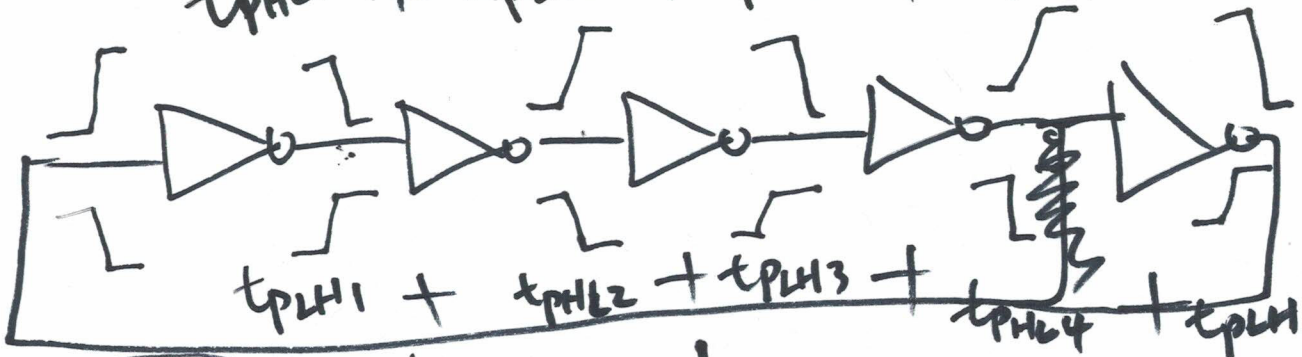


Δ Ring oscillator





$t_{PHL1} + t_{PLH2} + t_{PHL3} + t_{PLH4} + t_{PHL5} = \frac{1}{2}T$



$t_{PLH1} + t_{PHL2} + t_{PLH3} + t_{PHL4} + t_{PLH5} = \frac{1}{2}T$

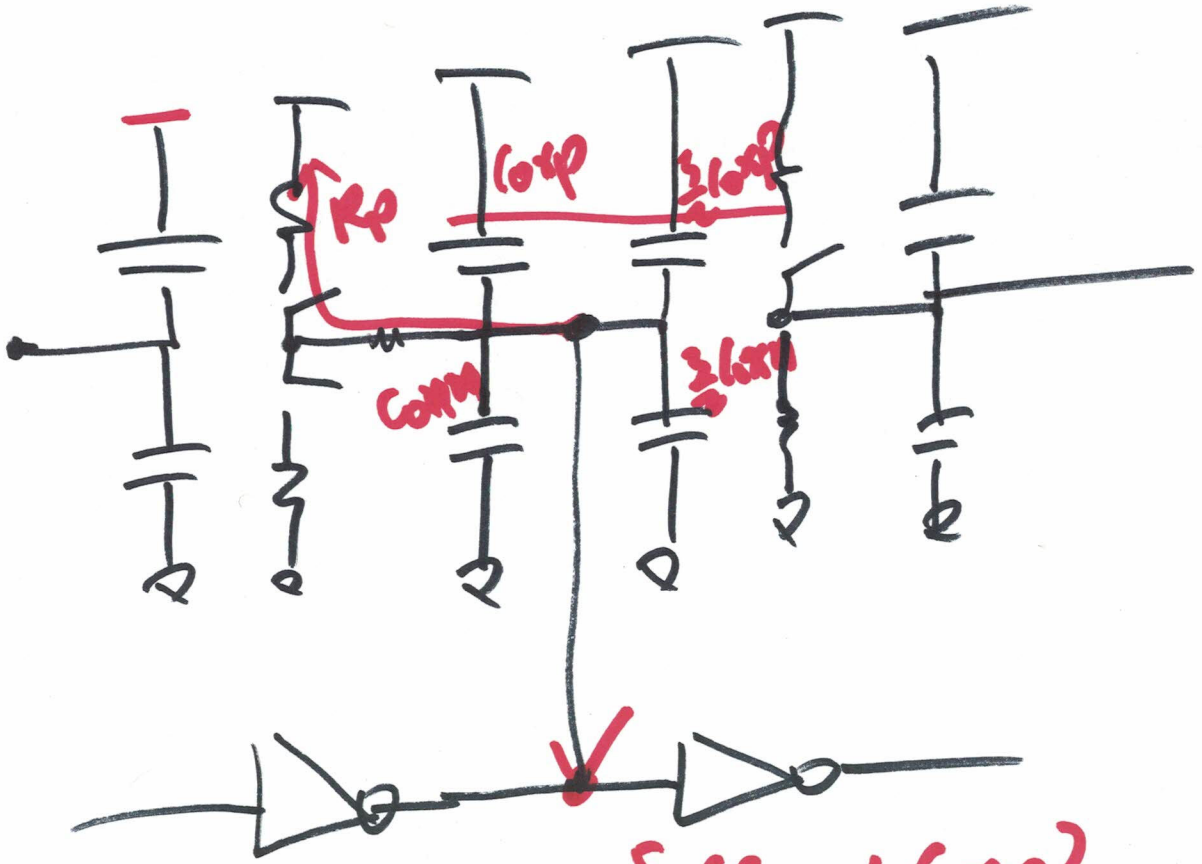
$+$

$\frac{1}{T} = f$

$\frac{1}{n(t_{PHL}+t_{PLH})} = f_{osc}$

$\frac{1}{T}$

(2)



$$t_{PLH} = 0.7 R_p \cdot \frac{5}{2}(C_{drn} + C_{drp})$$

$$t_{PHL} = 0.7 R_n \cdot \frac{5}{2}(C_{drn} + C_{drp})$$

a fosc of an 11-stage ring oscillator.

NMOS: $R_n = 3.4K$, $C_{ox}n = 0.6fF$

PMOS: $R_p = 3.4k$, $C_{ox}p = 1.25ff$

$$f_{osc} = \frac{1}{n(t_{pLH} + t_{pHL})}$$

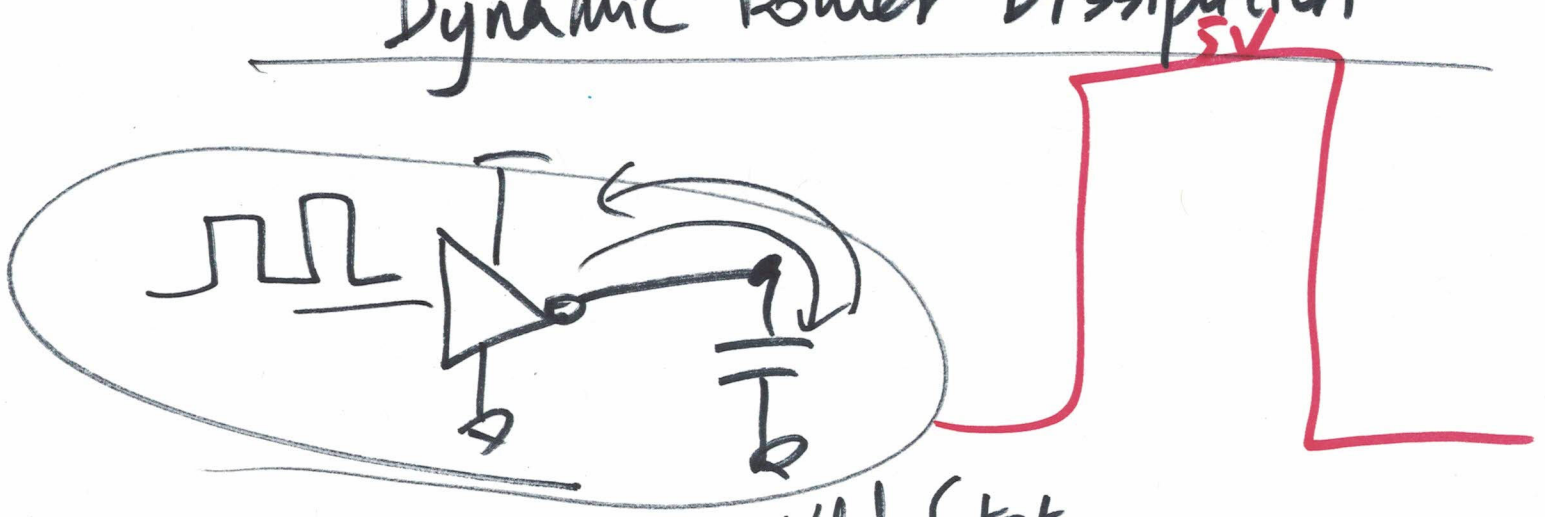
$C_{ox} = C_{ox}' \cdot A$

$$\begin{cases} t_{pLH} = 0.7 R_p \cdot \frac{5}{2}(C_{ox}n + C_{ox}p) \\ t_{pHL} = 0.7 R_n \cdot \frac{5}{2}(C_{ox}n + C_{ox}p) \end{cases}$$

$$f_{osc} = \frac{1}{11.22ps} = 4.16\,GHz$$

(4)

Dynamic Power Dissipation



$$I_{avg} = \frac{Q_{tot}}{T} = \frac{V_{dd} \cdot C_{tot}}{T}$$

$$P_{avg} = I_{avg} \cdot V_{dd} = V_{dd}^2 \cdot C_{tot} \cdot \frac{1}{T}$$

$$= V_{dd}^2 \cdot C_{tot} \cdot f$$

1.8V

$C_S \rightarrow 500\,nm$

$V_{dd} = 5V$

350 nm → TSMC 180 nm (1.8V)

50nm

Clocked Circuit

① A level-sensitive latch