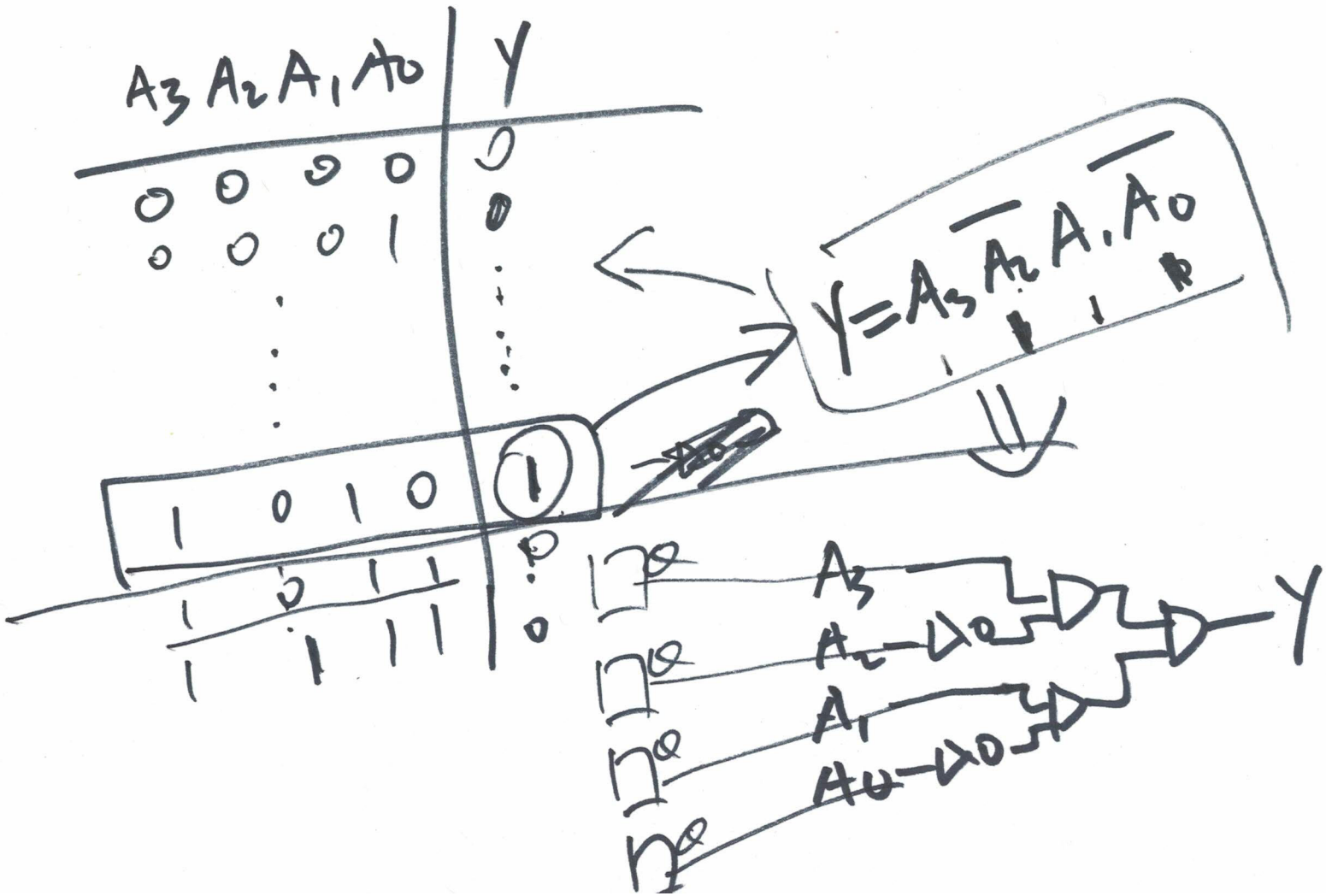
Combinational Digital Logic Design

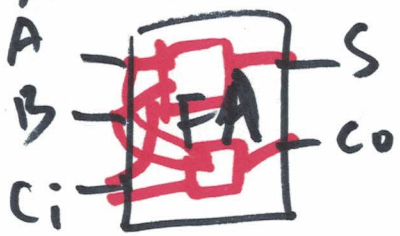
8-bit SAR ADC

count to 10 counter

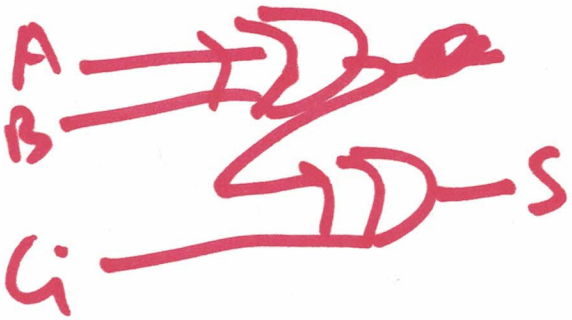


~~$B_2 B_1 B_0 + A_2 A_1 A_0$~~ High Speed Full Adder (FA)

~~B+A~~



A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



S_i

A \ BCi	00	01	11	10
0		1		1
1	1		1	

$$S = \bar{A}\bar{B}C_i + \bar{A}B\bar{C}_i + A\bar{B}\bar{C}_i + ABC_i$$

$$= (\bar{A}\bar{B} + AB)C_i + (A\bar{B} + \bar{A}B)\bar{C}_i$$

$$= (A \odot B)C_i + (A \oplus B)\bar{C}_i$$

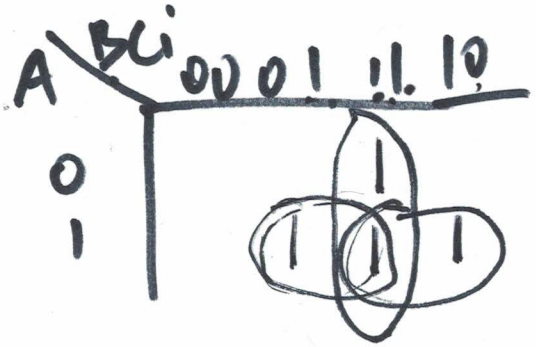
$$= \overline{(A \oplus B)} \cdot C_i + (A \oplus B)\bar{C}_i$$

$$= (A \oplus B) \oplus C_i$$

$$= A \oplus B \oplus C_i$$

(2)

C_0:

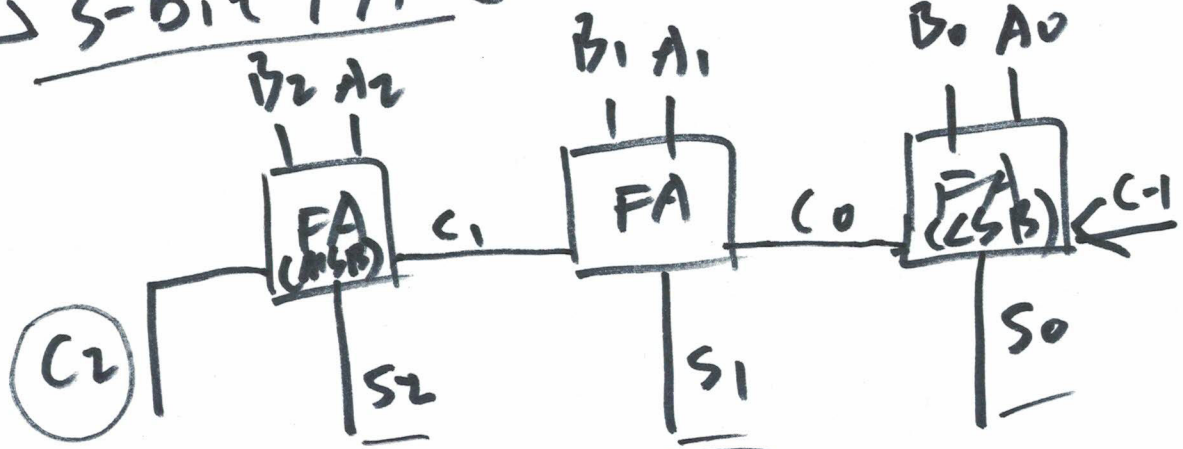


$$C_0 = BC_i + AC_i + AB$$
$$= (A+B)C_i + AB$$

$$\begin{array}{r} 1000 \quad -8 \\ +\ 1000 \quad -8 \\ \hline 10000 \quad -16 \end{array}$$

$$\begin{array}{r} B_2\ B_1\ B_0 \\ +\ A_2\ A_1\ A_0 \\ \hline 10 \end{array}$$

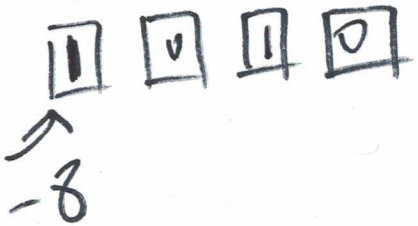
△ 3-bit FA (Ripple-carry Adder, RCA)

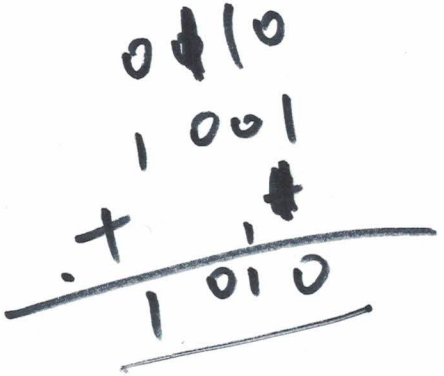


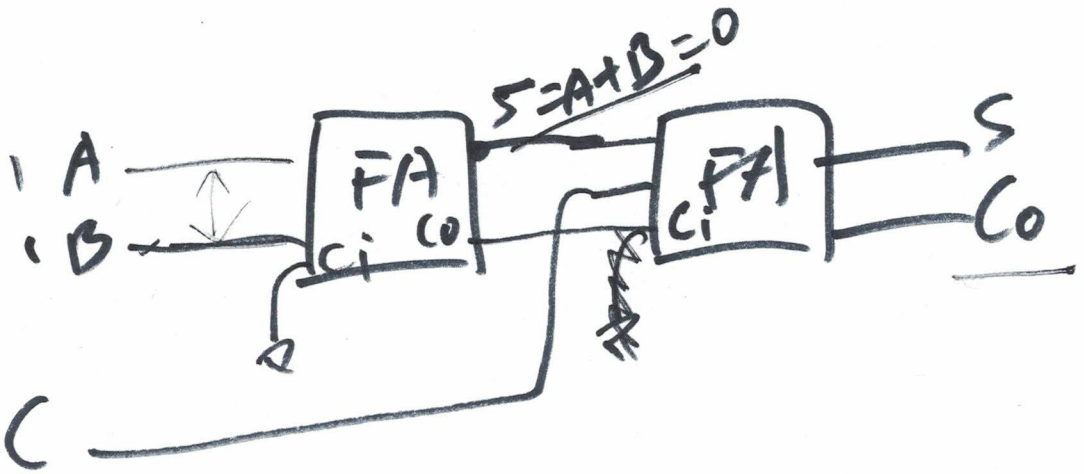
$C_2 S_2 S_1 S_0$

CE433

4-bit -6



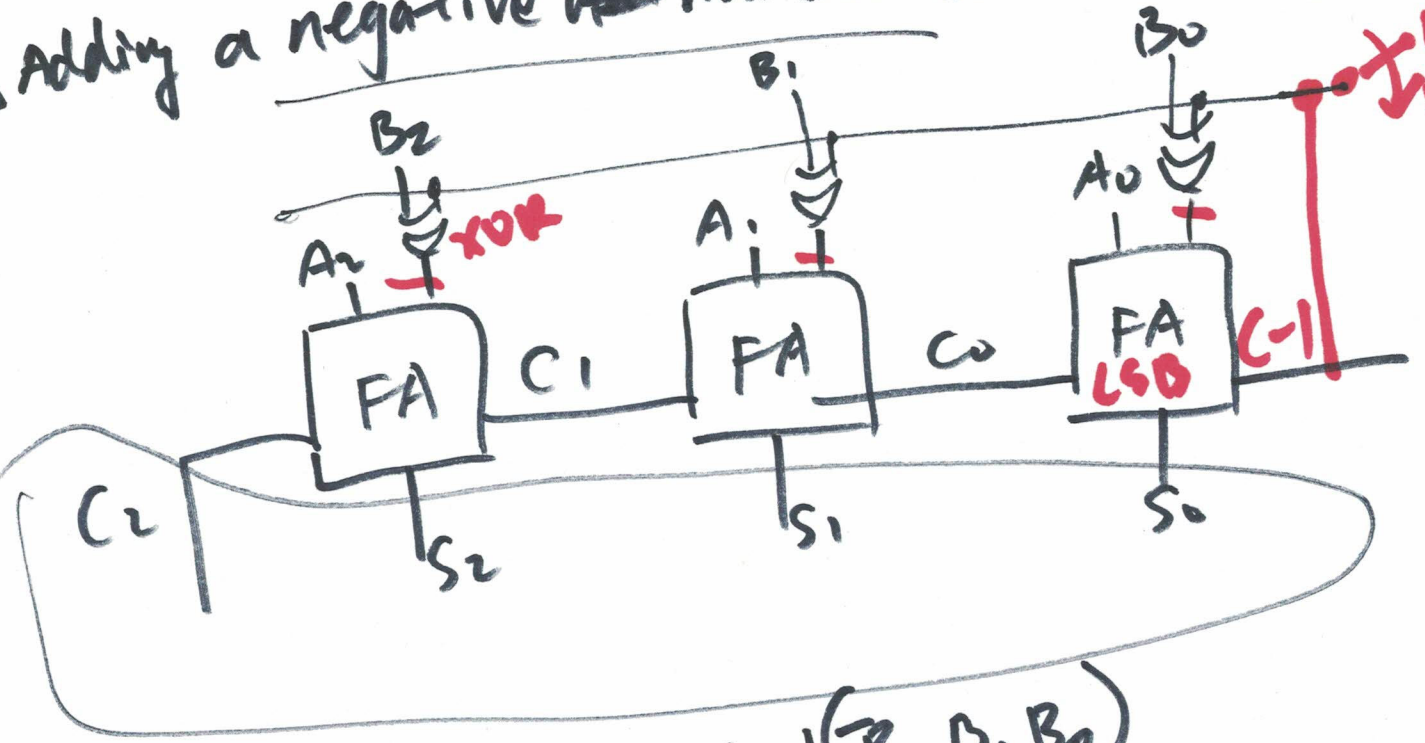




$B \oplus 1 = \bar{B}\cdot 1 + B\cdot\bar{1}$
$= \bar{B} + 0$
$= \bar{B}$

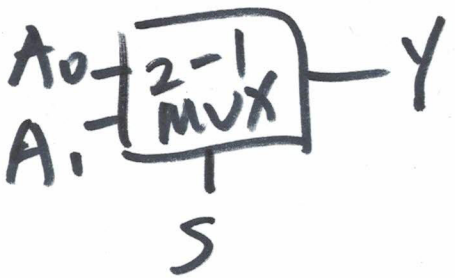
$B \oplus 0 = \bar{B}\cdot 0 + B\bar{0}$
$= 0 + B$
$= B$

△ Adding a negative number (subtraction)



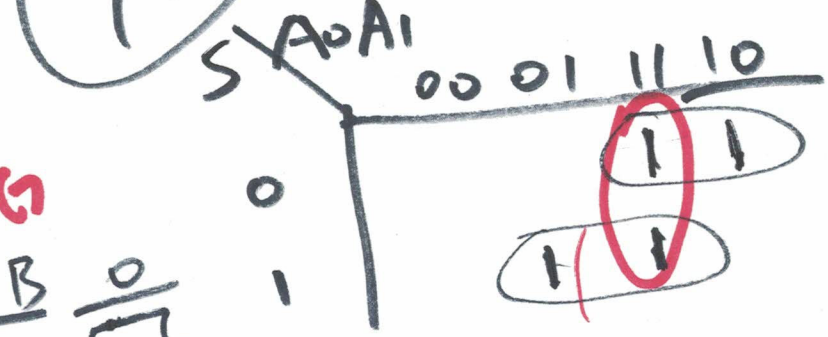
$A_2 A_1 A_0 + (B_2 B_1 B_0)$

MUX:



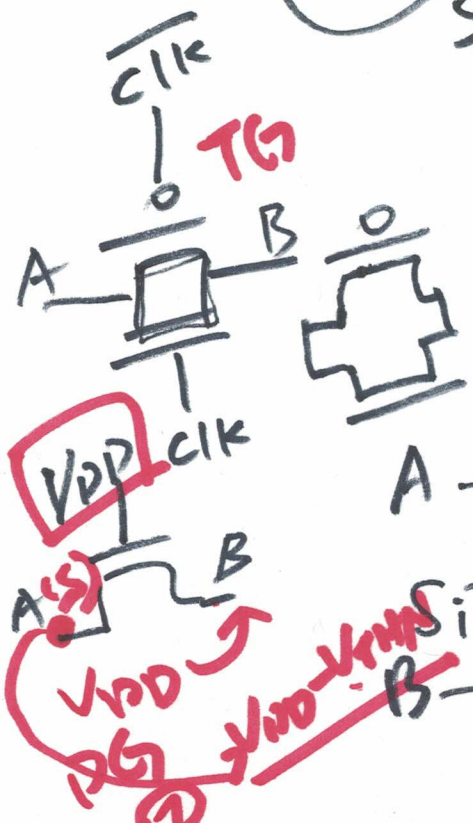
S	A0	A1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

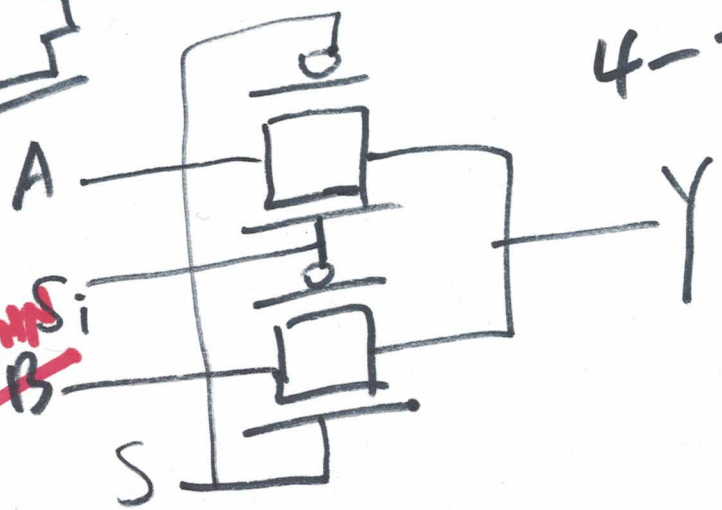
Y:



$$Y = \bar{S}A_0 + SA_1 + A_0A_1$$

too many gates





4-transistor circuit