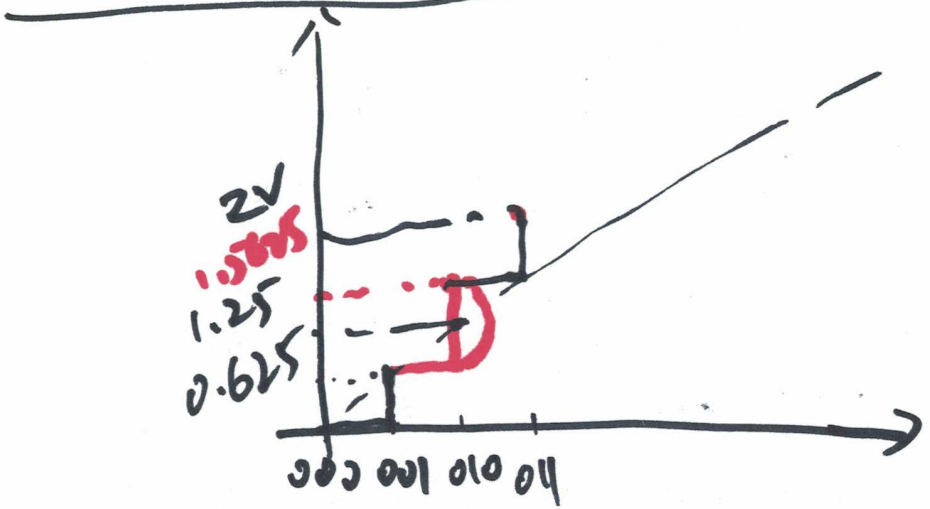
HW2 Review

Digital Input	Vout	Ideal Vout
000	0V	0V
001	0.625V	0.625V
010	1.5625V	1.25V
011	2V	1.875
100	2.5V	2.5
101	3.125V	3.125
→ 110	3.4375V	3.75
111	4.375V	4.375



$$DNL_2 = \frac{1.5625-0.625}{0.625} - 1LSB$$
$$= 0.5LSB$$

$$DNL_3 = \frac{2V-1.5625}{0.625} - 1LSB$$
$$= -0.3\,LSB$$

$$DNL_4 = \frac{2.5-2}{0.625} - 1LSB$$
$$= -0.2\,LSB$$

$$DNL_6 = \frac{3.4375-3.125}{0.625} - 1LSB$$
$$= -0.5\,LSB$$

$$DNL_7 = \frac{4.375-3.4375}{0.625} - 1LSB$$
$$= 0.5\,LSB$$

$$INL_2 = \frac{1.5625 - 1.25}{0.625} = 0.5\,LSB$$

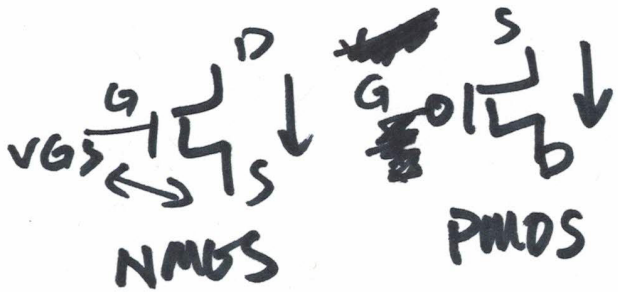
$$INL_3 = \frac{2 - 1.875}{0.625} = 0.2\,LSB$$

$$INL_6 = \frac{3.4375 - 3.75}{0.625} = -0.5\,LSB$$

~~INL_7~~

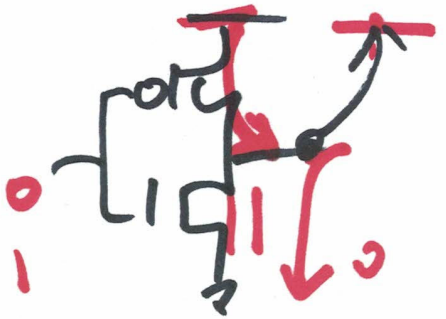
(2)

MOSFETs



CMOS

⟹ complementary



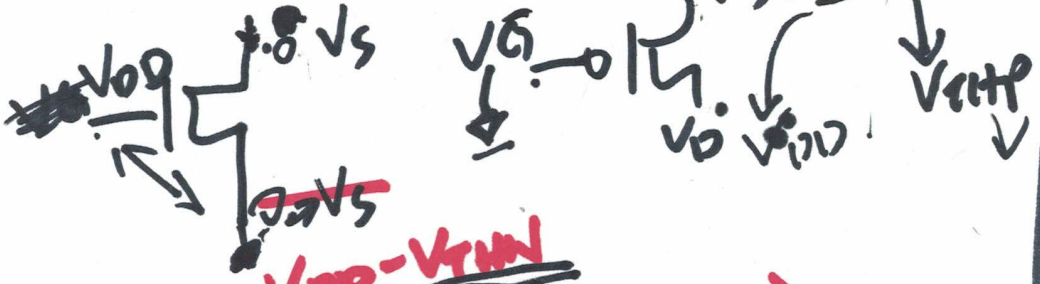
VGS ≥ VTHN

NMOS is good at passing 0's but not 1's.

VGS − VTHN ≥ 0

VSG ≥ VTHP

PMOS is good at passing 1's but not 0's

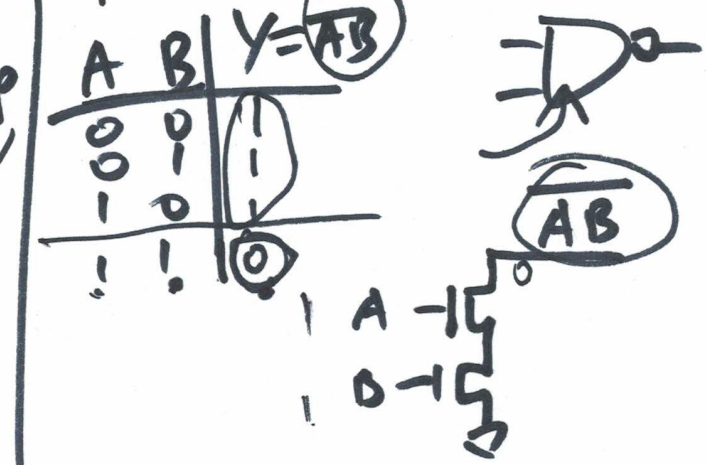


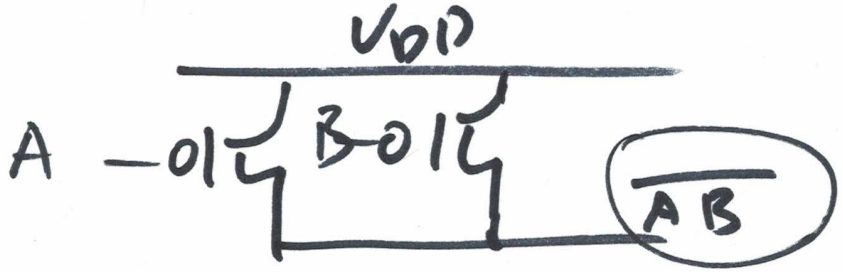
$V_{GS} = V_{DD} - (V_{DD} - V_{THN})$

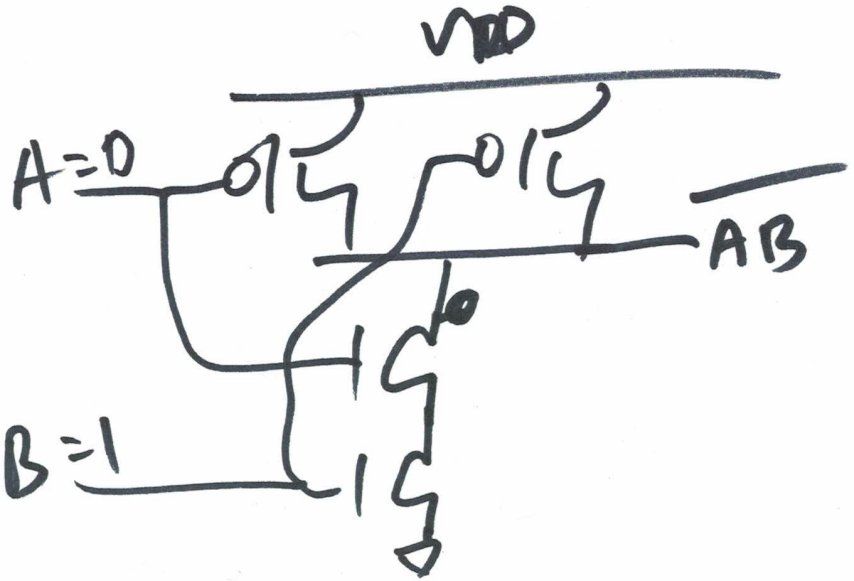
$= V_{DD} - V_{DD} + V_{THN}$

NAND

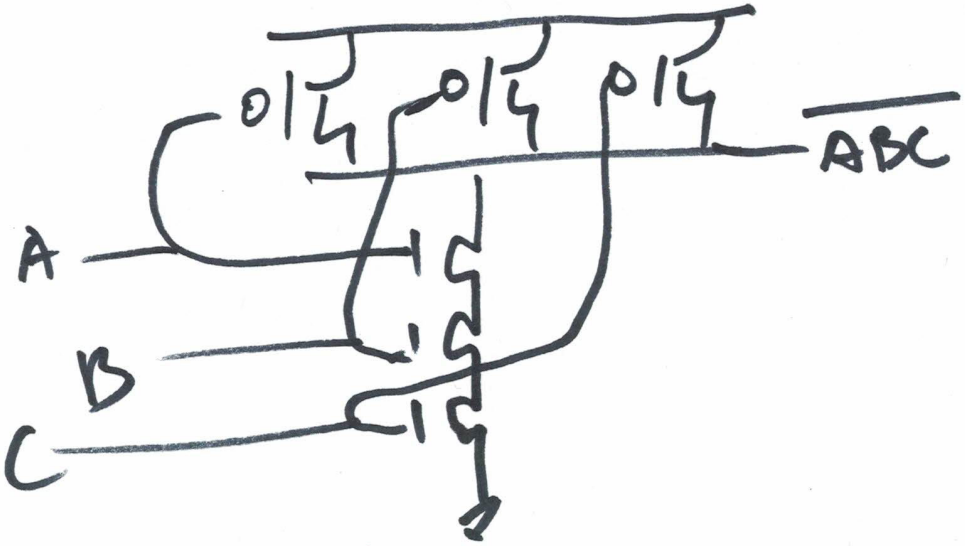
A	B	Y = $\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

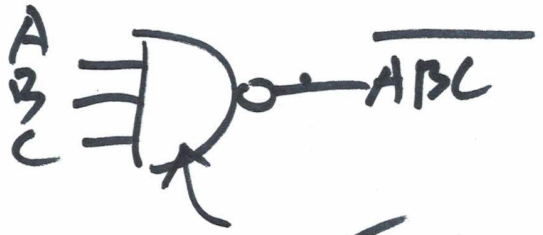


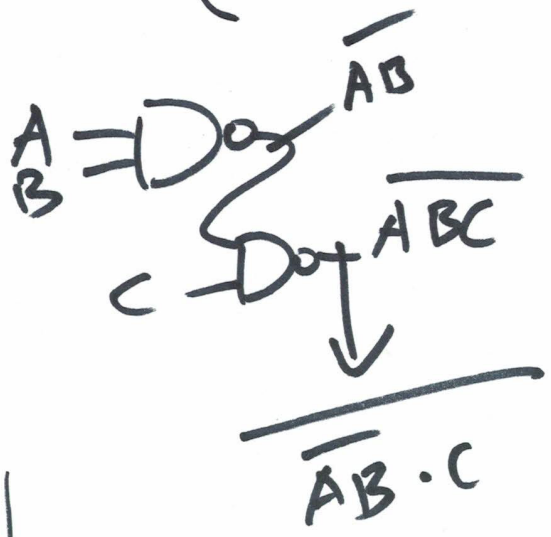

VDD
A
B
$\overline{AB}$


VDD
A=0
B=1
$\overline{AB}$

① $Y = \overline{A \cdot B \cdot C}$

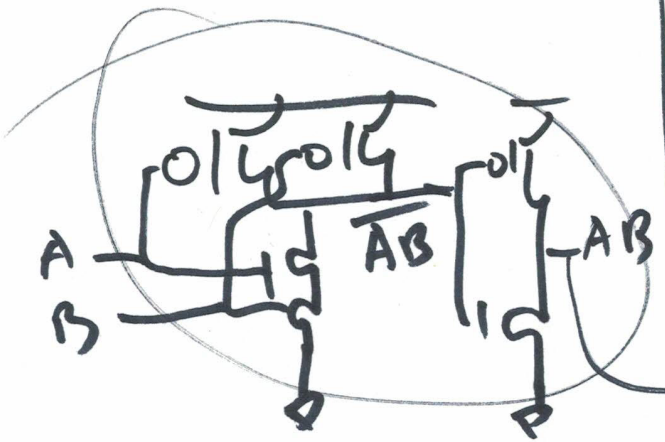


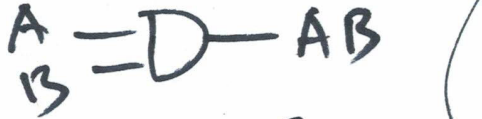


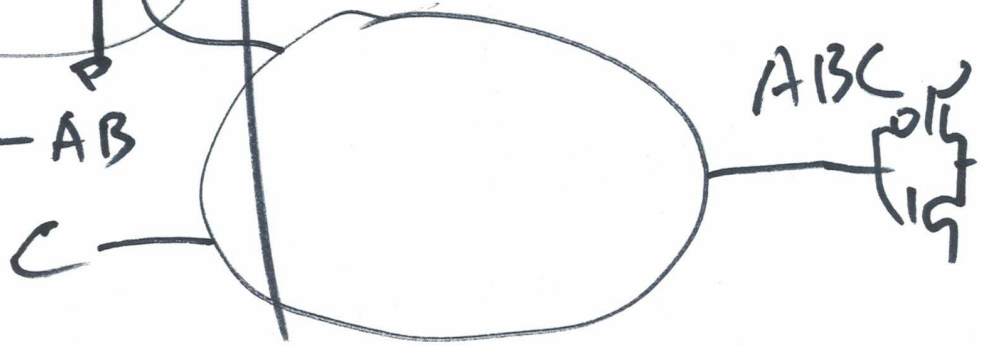


AOI Logic

AND
OR
Invert





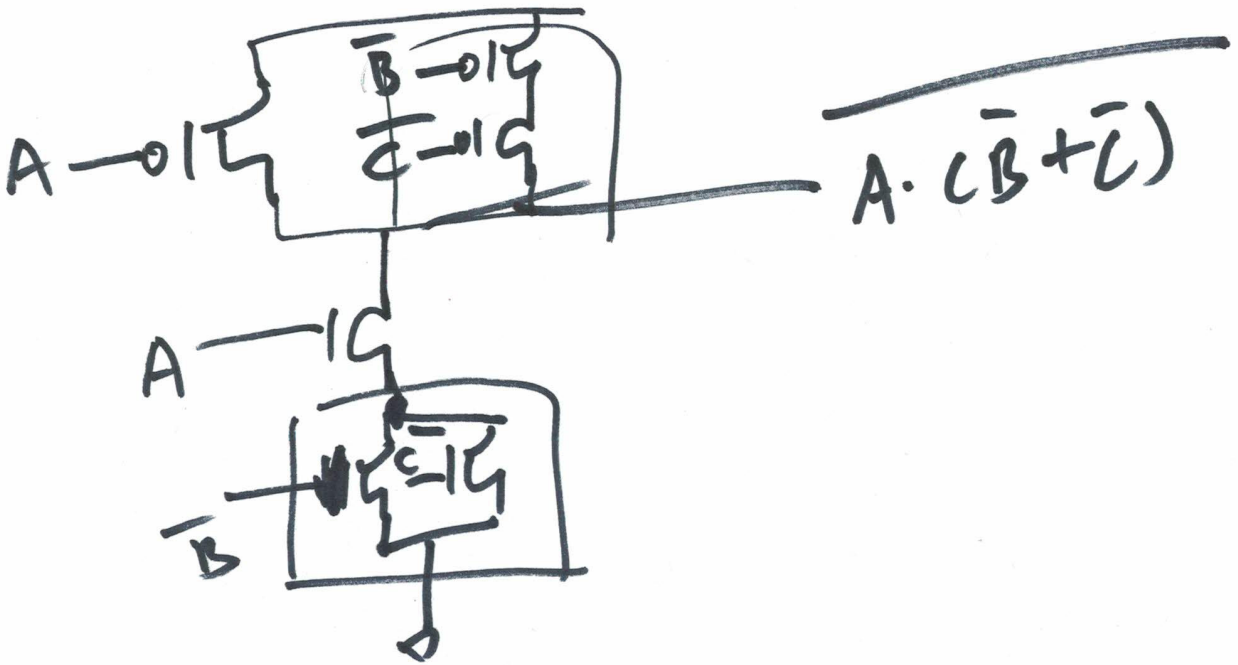


$$Y = \bar{A} + BC$$

$$= \overline{\bar{A} + BC}$$

$$= \bar{\bar{A}} \cdot \overline{BC}$$

$$= A \cdot (\bar{B} + \bar{C})$$



(b)