① always @ ( ) ;

② input {a, b, c};

output {a, b, c};

③ Hierarchical

module top;

~~orgate~~

orgate or_gate1 (....)

orgate or_gate2 (....)

endmodule

module AndGate( )

endmodule

module orgate ( );

. . .

. . . .

endmodule

- R_2R_DAC
  - R_2R_DAC.sch
  - R_2R_DAC.icn
  - R_2R_DAC.lay
- sim_R_2R_DAC.sch

④ structural

or or_gate1 (out, in1, in2);

⑤ Behavioral

~~reg~~ initial Q=0; unknown

begin

Q=0; outputs 0

end

only required if you have more than one lines of code

assign

```
res3 = num1;
```

```
res3[0] = num1[7]
res3[1] = num1[6]
   .
   .
   .
res3[7] = num1[0]
```

$A \oplus 0 = A$

$A \oplus 1 = \overline{A}$

$125_{(10)} \div 10 = 12.5$

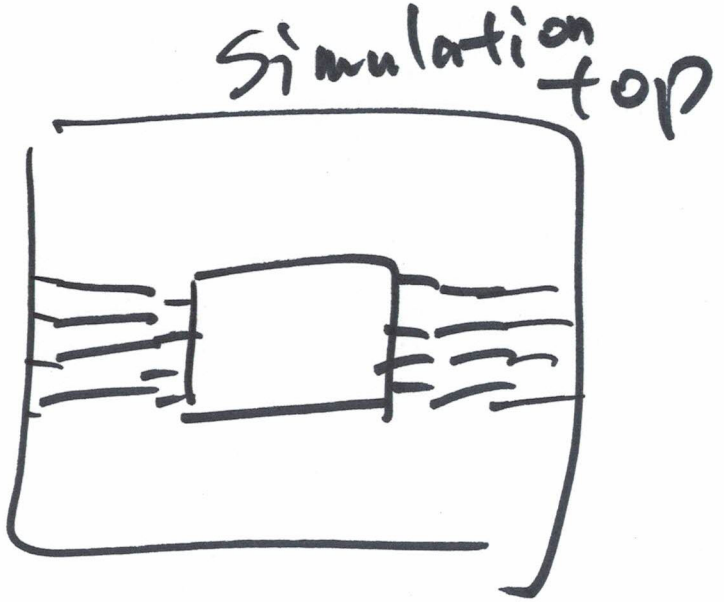
$\div 100 = 1.25$

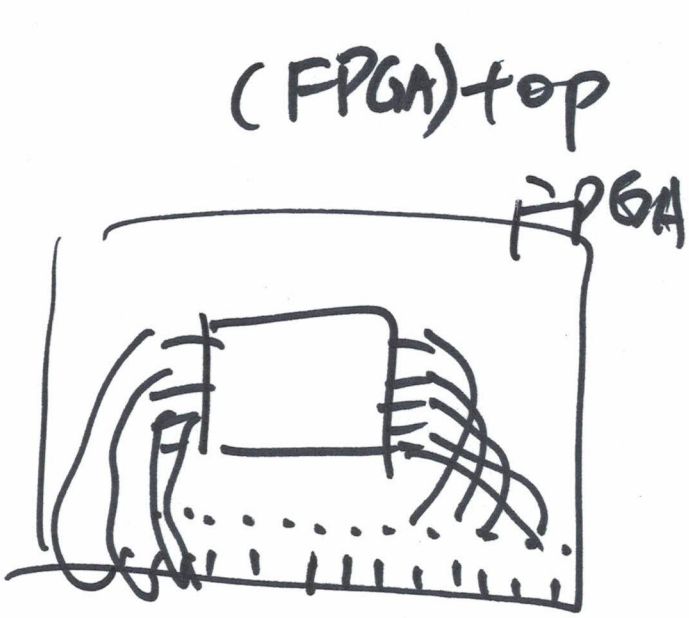
$1101._{(2)} \div 2 = 110.1$

$1101._{(2)} \times 2 = 1101.0$

$1101._{(2)} \div 4 = 11.01$

$0.00111 = 1.11 \times 2^{(-3)}$


Simulation top


(FPGA) top
FPGA