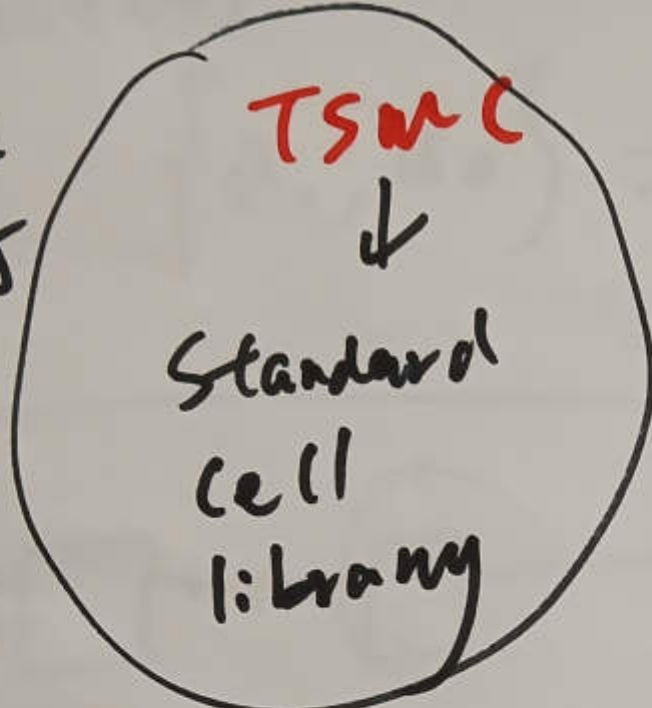
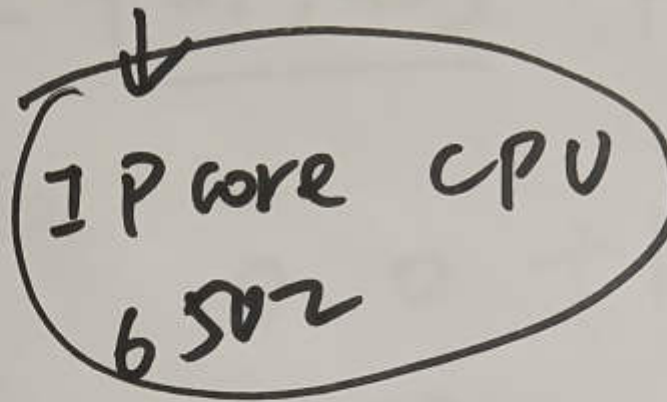


Pure plug

IP

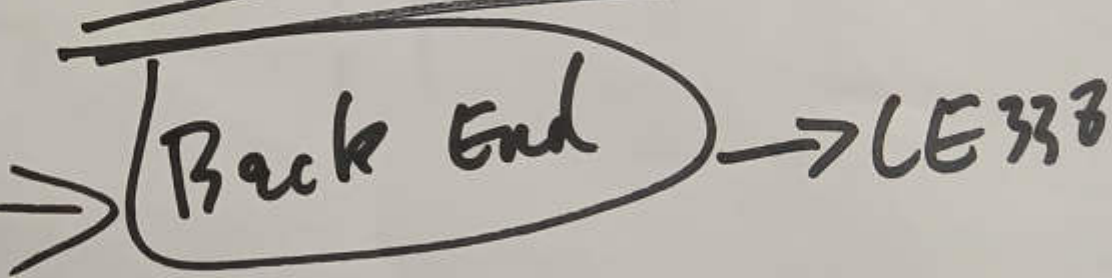


WDC



FPGA

Front End



Concatenation

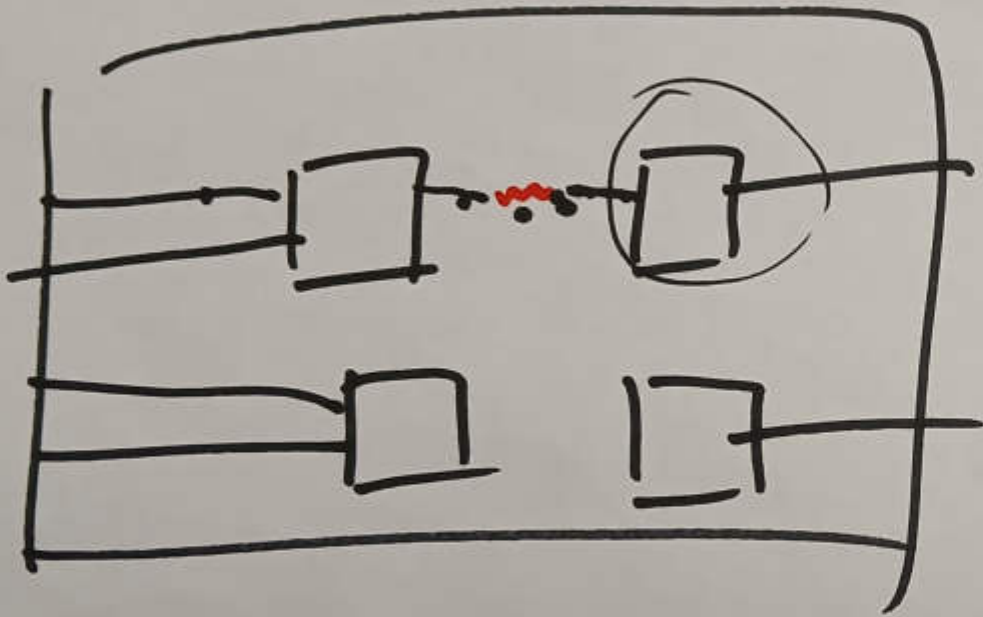
a<sub>0</sub>  
b<sub>0</sub>

$$\frac{\{ \overset{1}{b_0}, a_0 \}}{2\text{-bit}} + 1$$

①

repeat (4)

$$\{a_1, a_0\} = \underline{\{a_1, a_0\}} + 1$$



$$\begin{matrix} 0 & 0 & +1 \\ 0 & 0 & \\ 0 & 1 & \\ \vdots & 0 & \\ \vdots & 1 & \end{matrix}$$