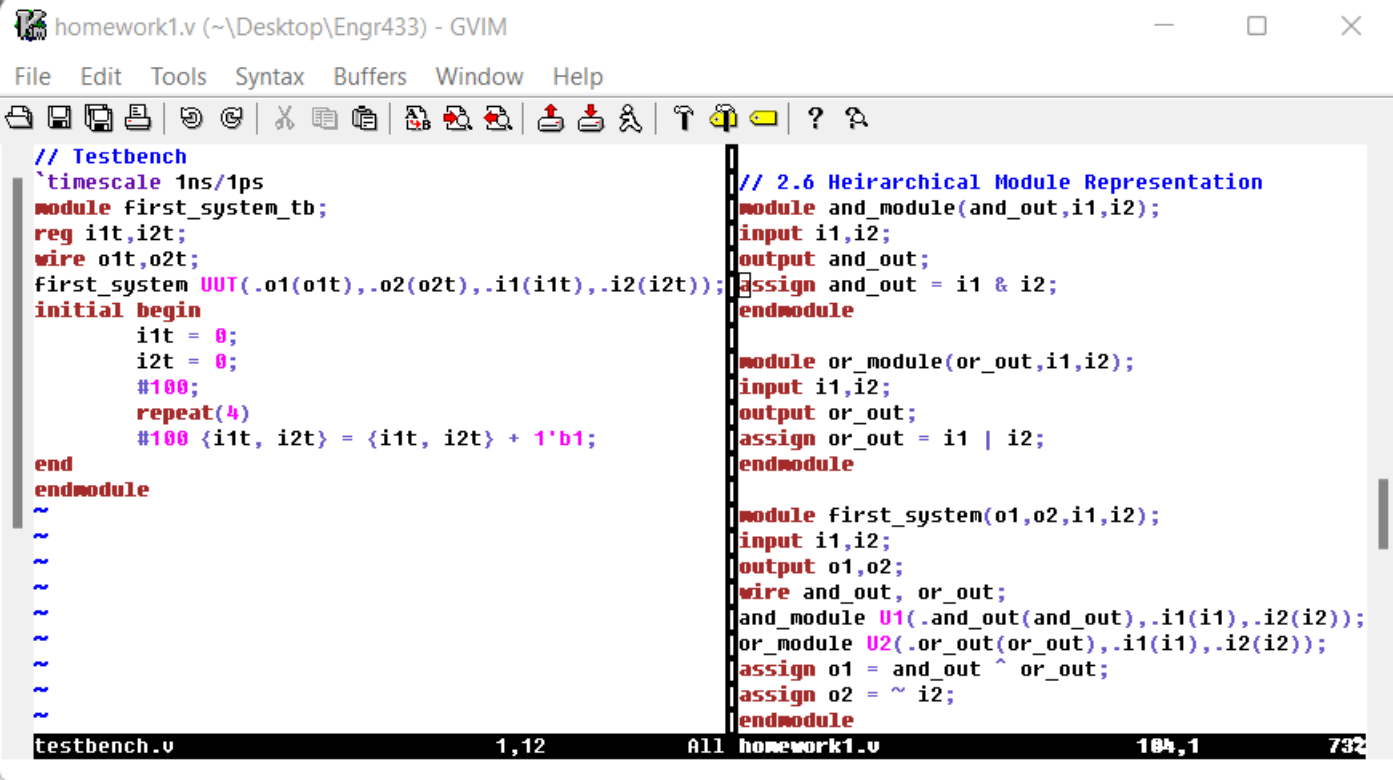
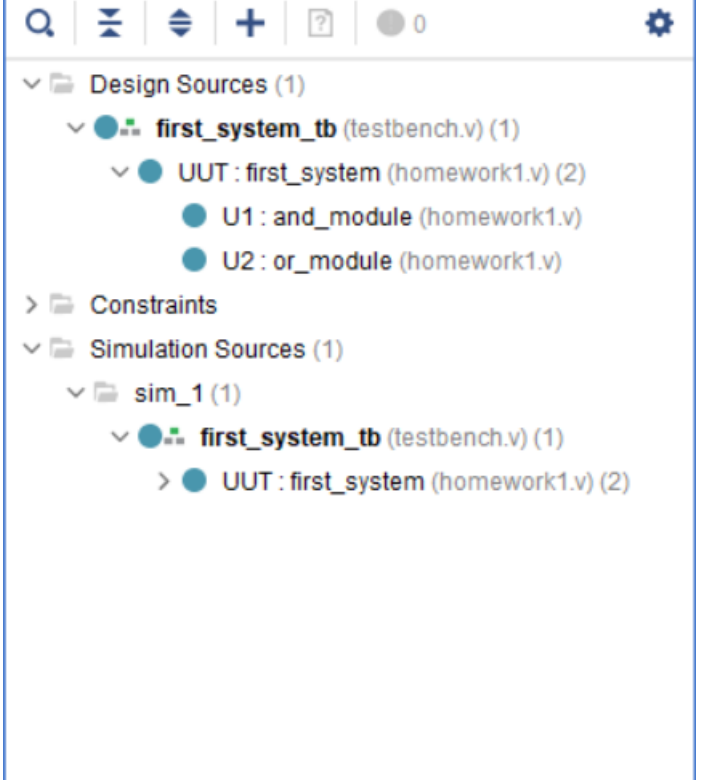
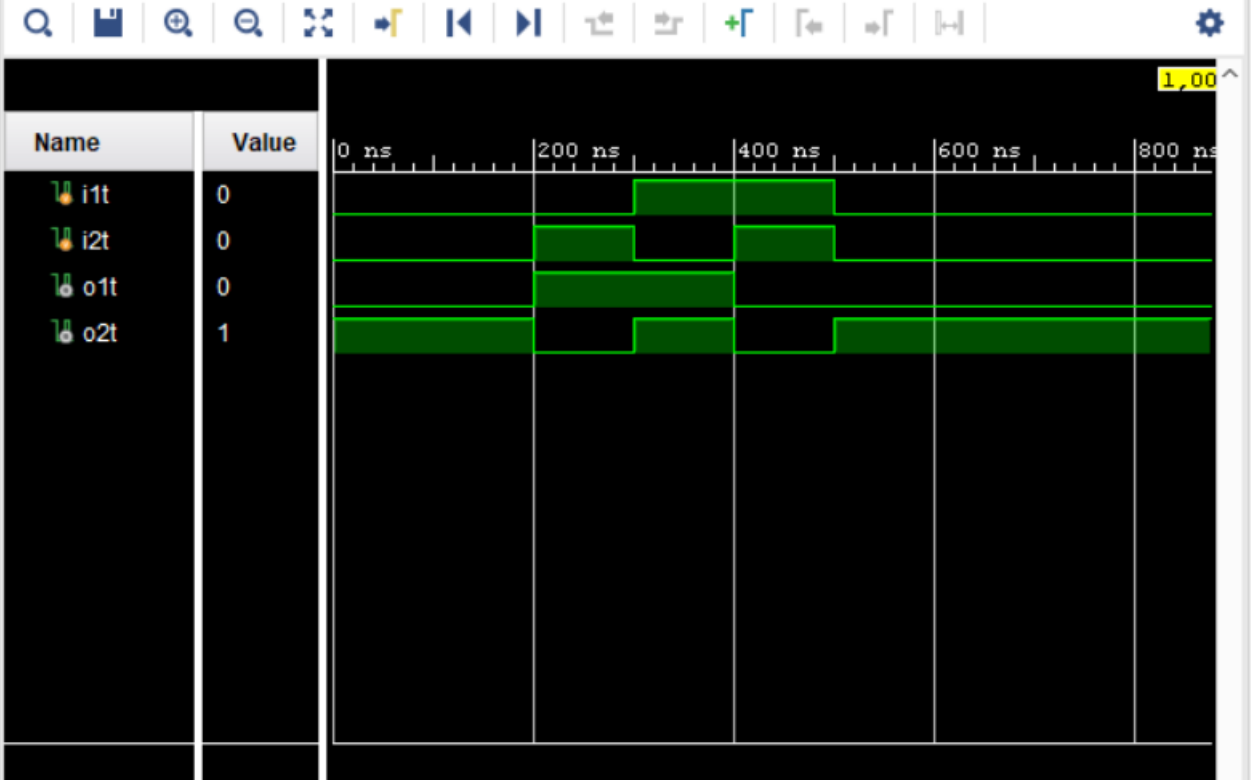

homework1.v (~\Desktop\Engr433) - GVIM
File Edit Tools Syntax Buffers Window Help
// Testbench
`timescale 1ns/1ps
module first_system_tb;
reg i1t,i2t;
wire o1t,o2t;
first_system UUT(.o1(o1t),.o2(o2t),.i1(i1t),.i2(i2t));
initial begin
i1t = 0;
i2t = 0;
#100;
repeat(4)
#100 {i1t, i2t} = {i1t, i2t} + 1'b1;
end
endmodule
testbench.v 1,12 All
// 2.6 Heirarchical Module Representation
module and_module(and_out,i1,i2);
input i1,i2;
output and_out;
assign and_out = i1 & i2;
endmodule
module or_module(or_out,i1,i2);
input i1,i2;
output or_out;
assign or_out = i1 | i2;
endmodule
module first_system(o1,o2,i1,i2);
input i1,i2;
output o1,o2;
wire and_out, or_out;
and_module U1(.and_out(and_out),.i1(i1),.i2(i2));
or_module U2(.or_out(or_out),.i1(i1),.i2(i2));
assign o1 = and_out ^ or_out;
assign o2 = ~ i2;
endmodule
homework1.v 104,1 732


0
Design Sources (1)
first_system_tb (testbench.v) (1)
UUT : first_system (homework1.v) (2)
U1 : and_module (homework1.v)
U2 : or_module (homework1.v)
Constraints
Simulation Sources (1)
sim_1 (1)
first_system_tb (testbench.v) (1)
UUT : first_system (homework1.v) (2)


Name
Value
i1t
0
i2t
0
o1t
0
o2t
1
0 ns
200 ns
400 ns
600 ns
800 ns
1,00