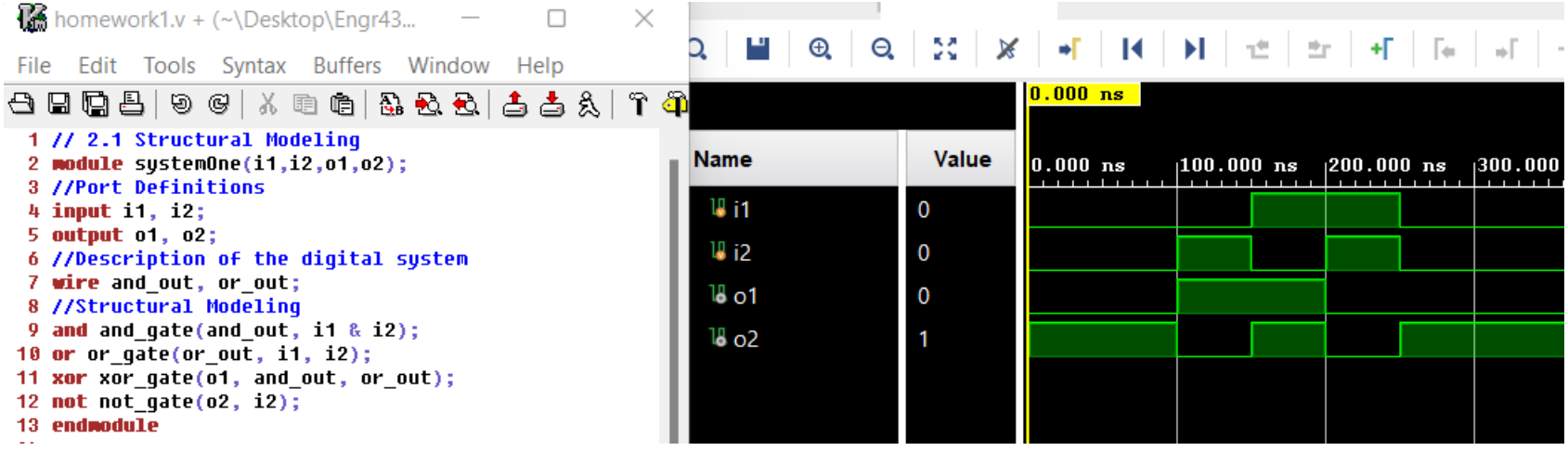
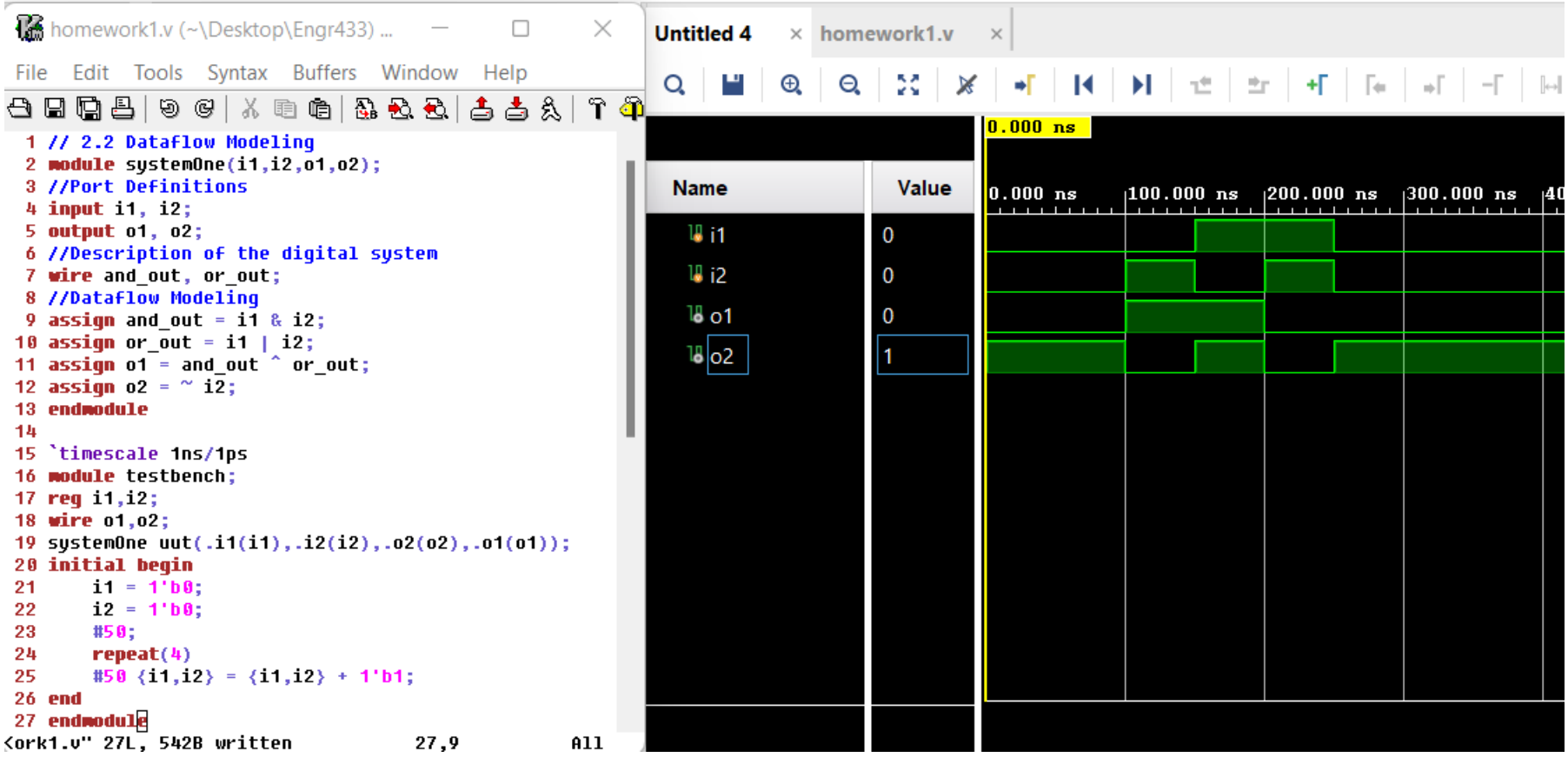

homework1.v + (~\Desktop\Engr43...
File Edit Tools Syntax Buffers Window Help
1 // 2.1 Structural Modeling
2 module systemOne(i1,i2,o1,o2);
3 //Port Definitions
4 input i1, i2;
5 output o1, o2;
6 //Description of the digital system
7 wire and_out, or_out;
8 //Structural Modeling
9 and and_gate(and_out, i1 & i2);
10 or or_gate(or_out, i1, i2);
11 xor xor_gate(o1, and_out, or_out);
12 not not_gate(o2, i2);
13 endmodule
Name
Value
i1
0
i2
0
o1
0
o2
1
0.000 ns
0.000 ns
100.000 ns
200.000 ns
300.000


homework1.v (~\Desktop\Engr433) ...
File Edit Tools Syntax Buffers Window Help
1 // 2.2 Dataflow Modeling
2 module systemOne(i1,i2,o1,o2);
3 //Port Definitions
4 input i1, i2;
5 output o1, o2;
6 //Description of the digital system
7 wire and_out, or_out;
8 //Dataflow Modeling
9 assign and_out = i1 & i2;
10 assign or_out = i1 | i2;
11 assign o1 = and_out ^ or_out;
12 assign o2 = ~ i2;
13 endmodule
14
15 `timescale 1ns/1ps
16 module testbench;
17 reg i1,i2;
18 wire o1,o2;
19 systemOne uut(.i1(i1),.i2(i2),.o2(o2),.o1(o1));
20 initial begin
21 i1 = 1'b0;
22 i2 = 1'b0;
23 #50;
24 repeat(4)
25 #50 {i1,i2} = {i1,i2} + 1'b1;
26 end
27 endmodule
ork1.v" 27L, 542B written 27,9 All
Untitled 4
homework1.v
Name
Value
i1
0
i2
0
o1
0
o2
1
0.000 ns
0.000 ns
100.000 ns
200.000 ns
300.000 ns

homework1.v (~\Desktop\Engr433) ...

File Edit Tools Syntax Buffers Window Help

```
//assign o1 = and_out ^ or_out;
//assign o2 = ~ i2;
//endmodule

// 2.3 Behavioral Modeling
module systemOne(i1, i2, o1, o2);
//Port Definitions
input i1, i2;
output o1, o2;
//Description of the Digital System through
//Behavioral Modeling
reg o1, o2; // register type for holding values
initial // Initializing the system
begin
        o1 = 0;
        o2 = 0;
end
always @ (i1,i2) // Defining the behavior of the system
begin
        o1 = (i1 & i2) ^ (i1 | i2);
        o2 = ~ i2;
end
endmodule

// Testbench
`timescale 1ns/1ps
module testbench;
reg i1,i2;
wire o1,o2;
systemOne uut(.i1(i1),.i2(i2),.o2(o2),.o1(o1));
initial
begin
    i1 = 0;
    i2 = 0;
    #50;
    repeat(4)
    #50 {i1,i2} = {i1,i2} + 1'b1;
end
endmodule
```

63,9 Bot

Default Layout

homework1.v | Untitled 2