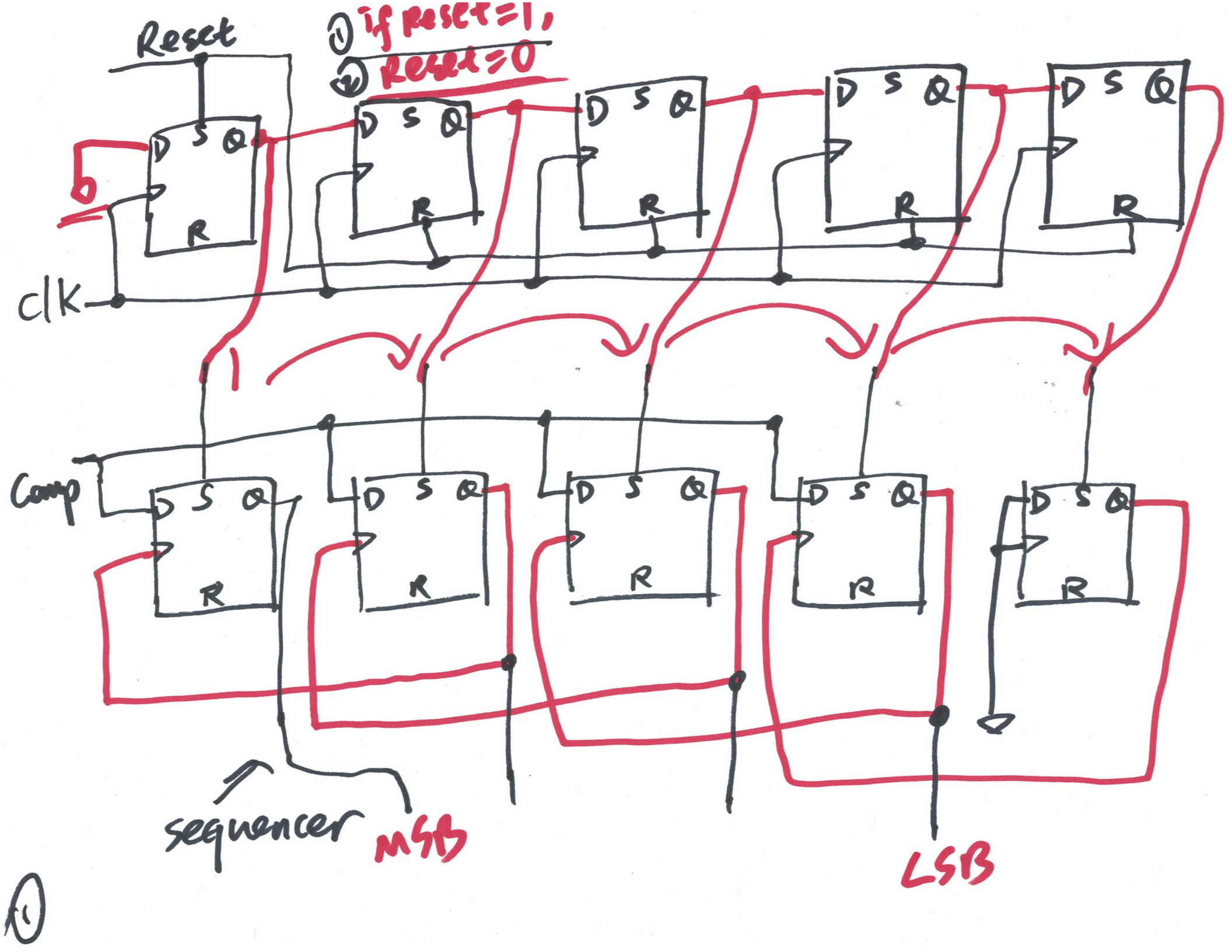
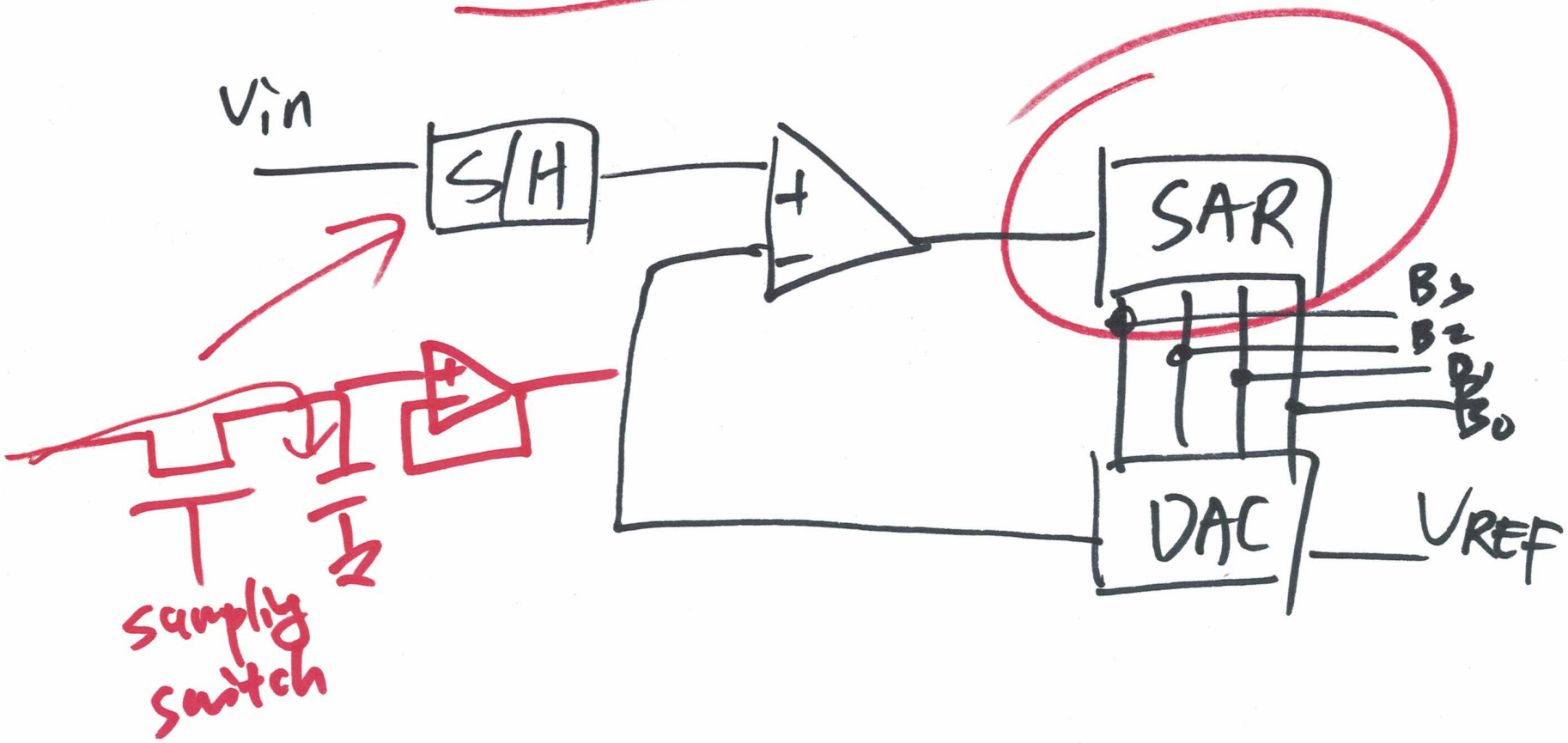

Reset
① if Reset=1,
② Reset=0
D S Q
R
clk
Comp
sequencer
MSB
LSB

SAR ADC



1.1 $-50^{\circ}C \rightarrow 150^{\circ}C \quad 0.1\,^{\circ}C$

$$\frac{150-(-50)+1}{0.1\,^{\circ}C} = 2010 \text{ steps}$$

$$2^N = 2010$$

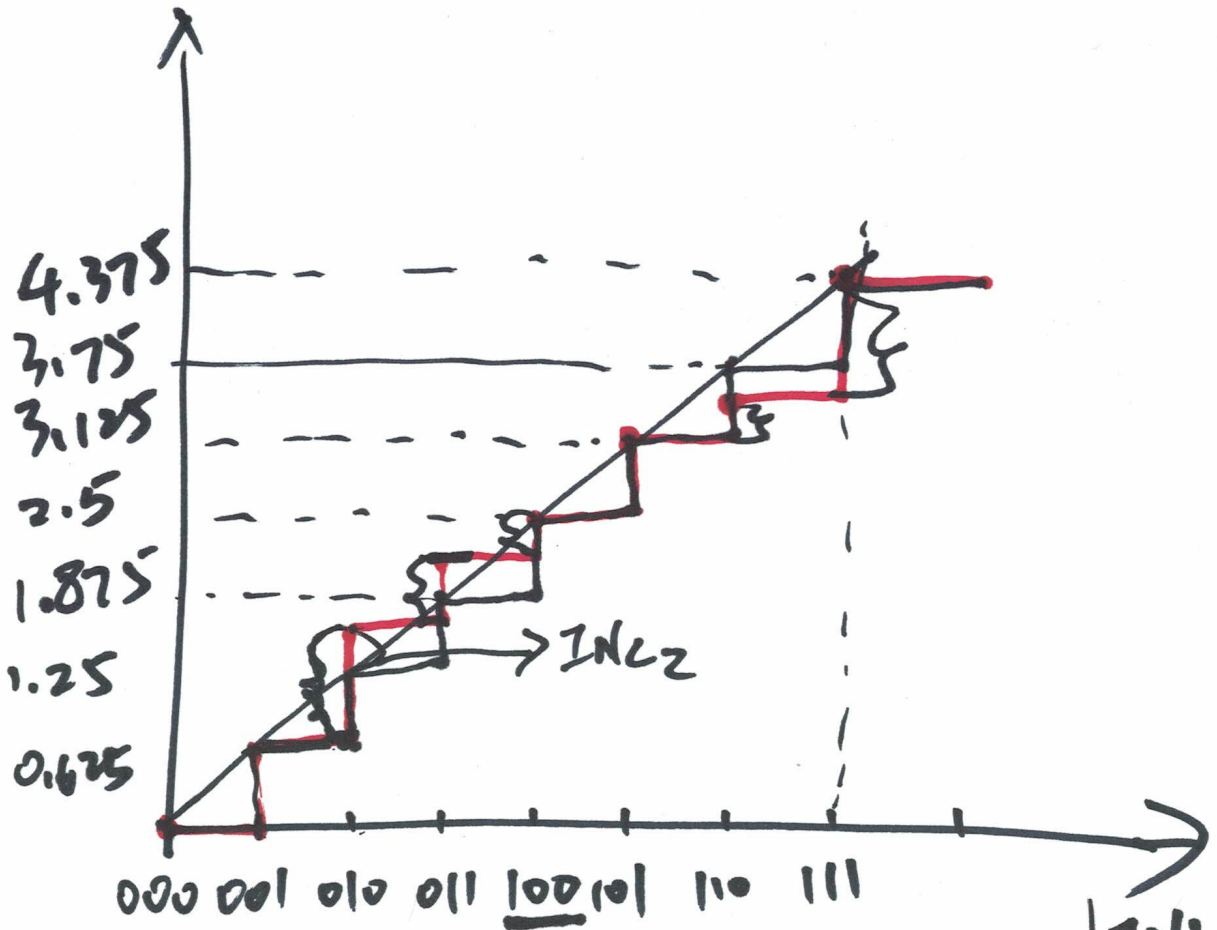
$$N = \log_2 2010 =$$

1.2 $$\frac{2^{N}-1}{2^{N}} = V_{FS}$$

3 bit DAC

Digital Input	Voltage Output	Ideal output
000	0	0
001	0.625	0.625
010	1.5625	1.25
011	2.0	1.875
100	2.5	2.5
101	3.125	3.125
110	3.4375	3.75
111	4.375	4.375

$2^3 \cdot 0.625 = V_{REF} = 5V$



$$DNL_2 = \frac{1.5625 - 0.625}{0.625} - 1LSB = 0.5LSB$$

$$DNL_3 = \frac{2 - 1.5625}{0.625} - 1LSB = -0.3LSB$$

$$DNL_4 = \frac{2.5 - 2}{0.625} - 1LSB = -0.5LSB$$

$DNL_6 = \ldots$

$DNL_7 = \ldots$

$$INL_2 = \frac{1.5625 - 1.25}{0.625} - 1LSB$$

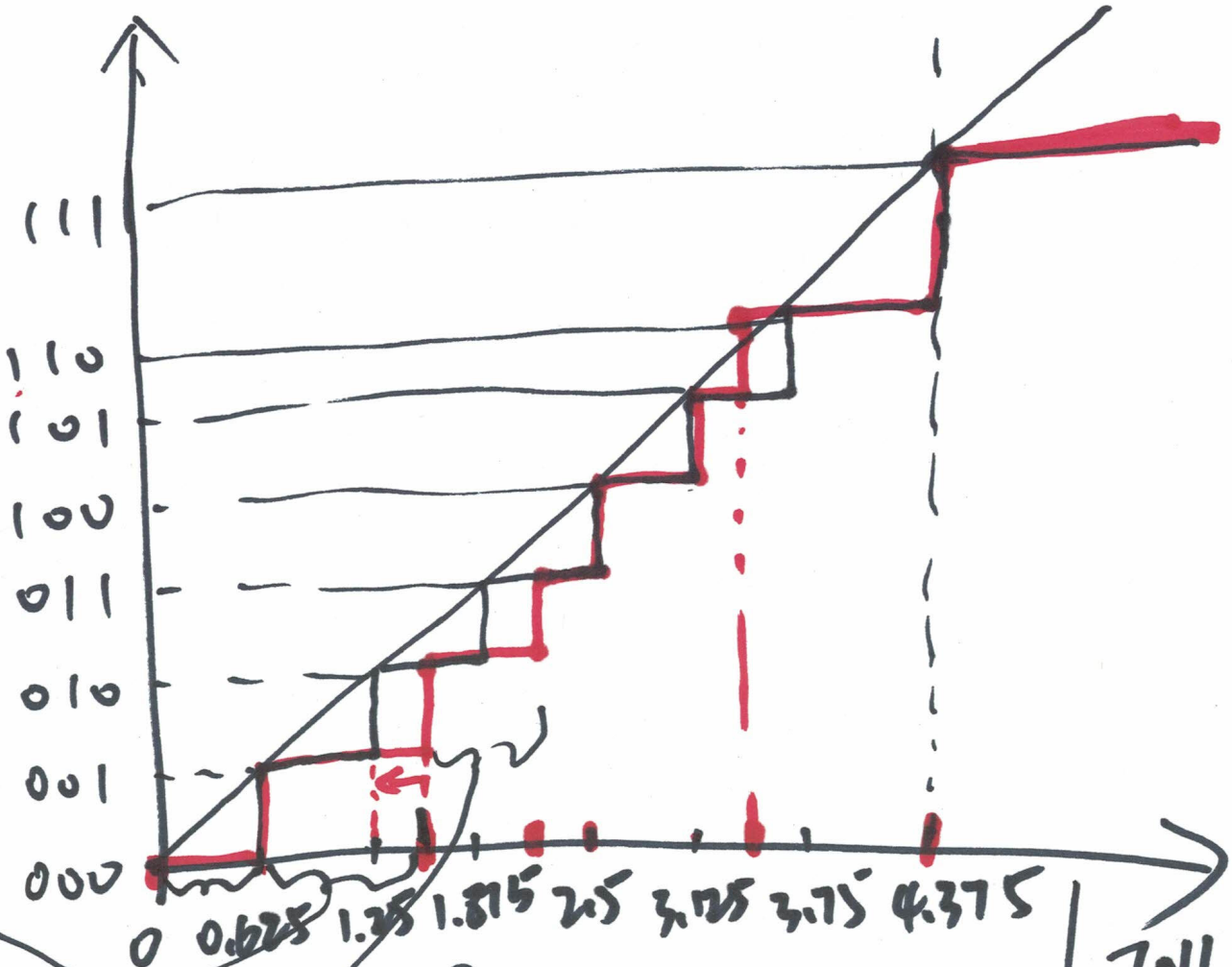
$$= 0.5LSB$$

(5)

3-bit ADC

Analog Input	Digital Output	Ideal Input
0	000	0
0.625	001	0.625
1.5625	010	1.25
2.0	011	1.875
2.5	100	2.5
3.125	101	3.125
3.4375	110	3.75
4.375	111	4.375

(b)



$$DNL_1 = \frac{1.5625 - 0.625}{0.625} - 1LSB = 0.5LSB$$

DNL_2

$$INL_2 = \frac{1.5625 - 1.25}{0.625} - 1LSB = 0.5LSB$$