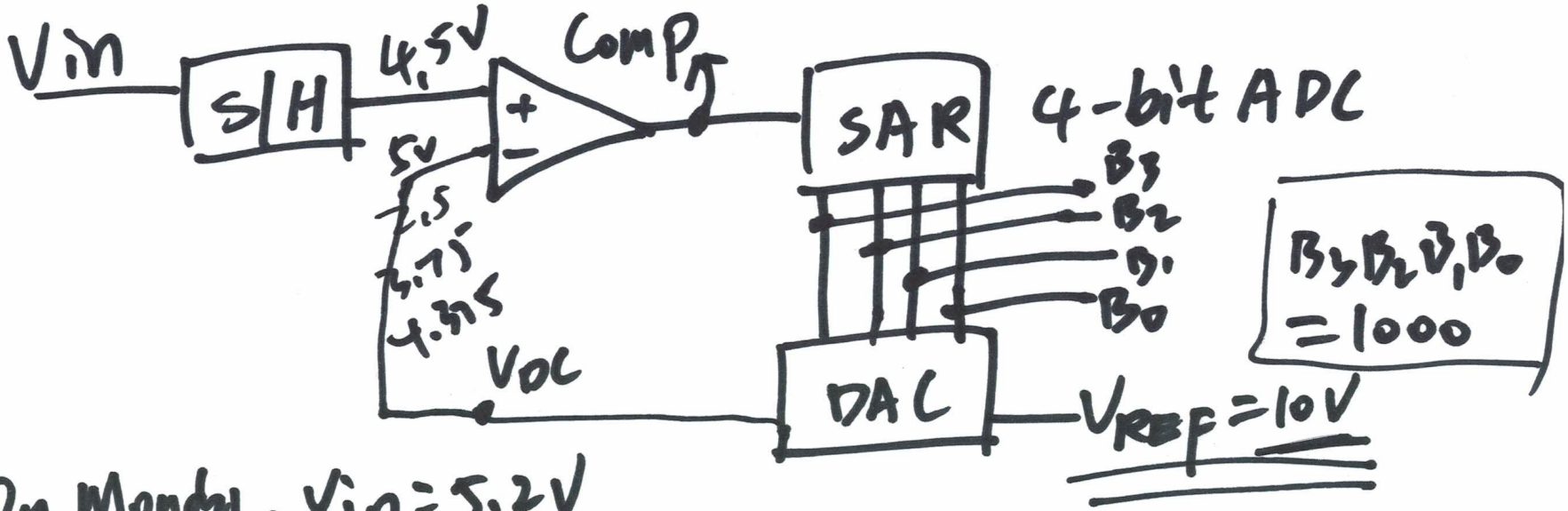
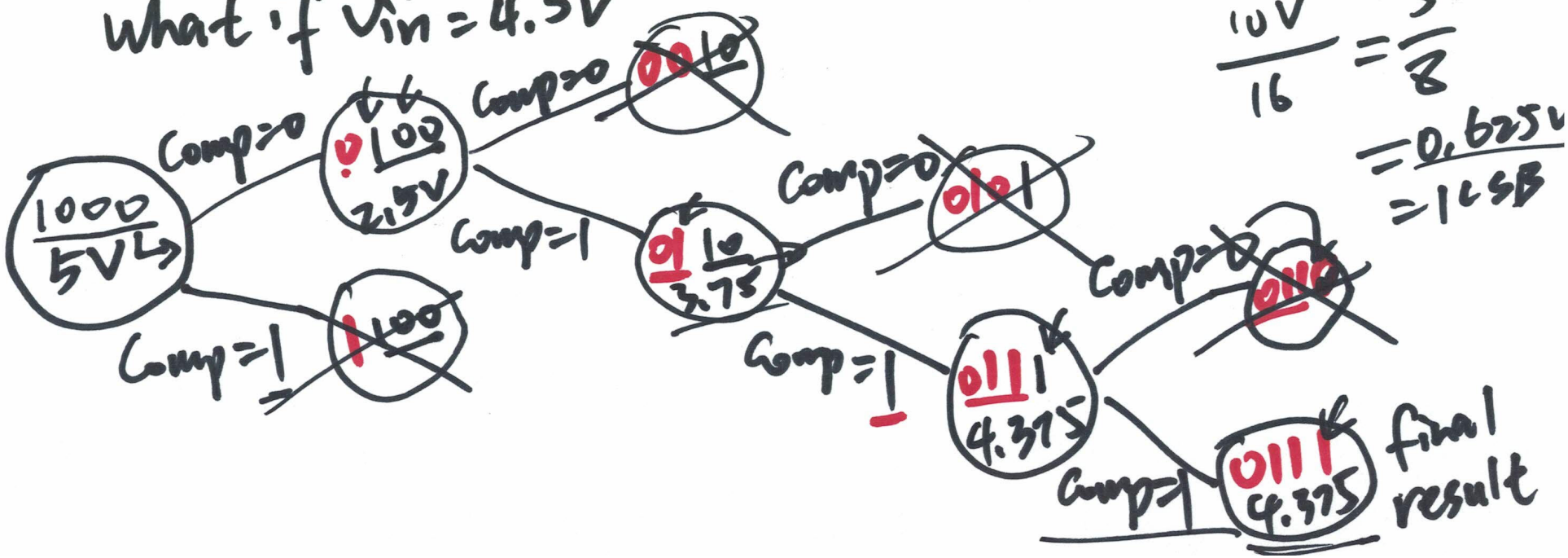
Successive Approximation Register ADC (SAR)



On Monday, $V_{in} = 5.2V$.

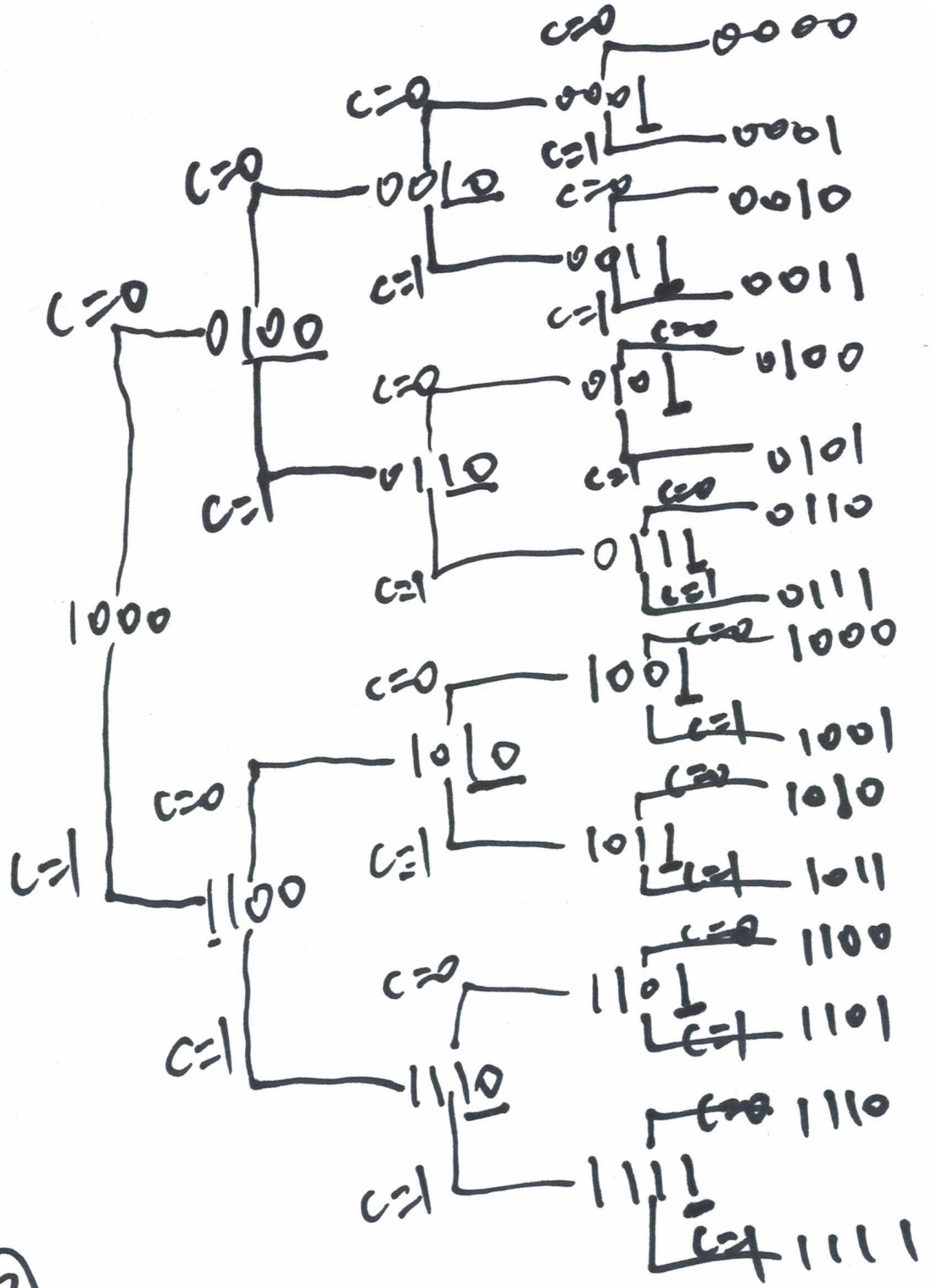
What if $V_{in} = 4.5V$



① N-bit SAR ADC, there are N+1 states

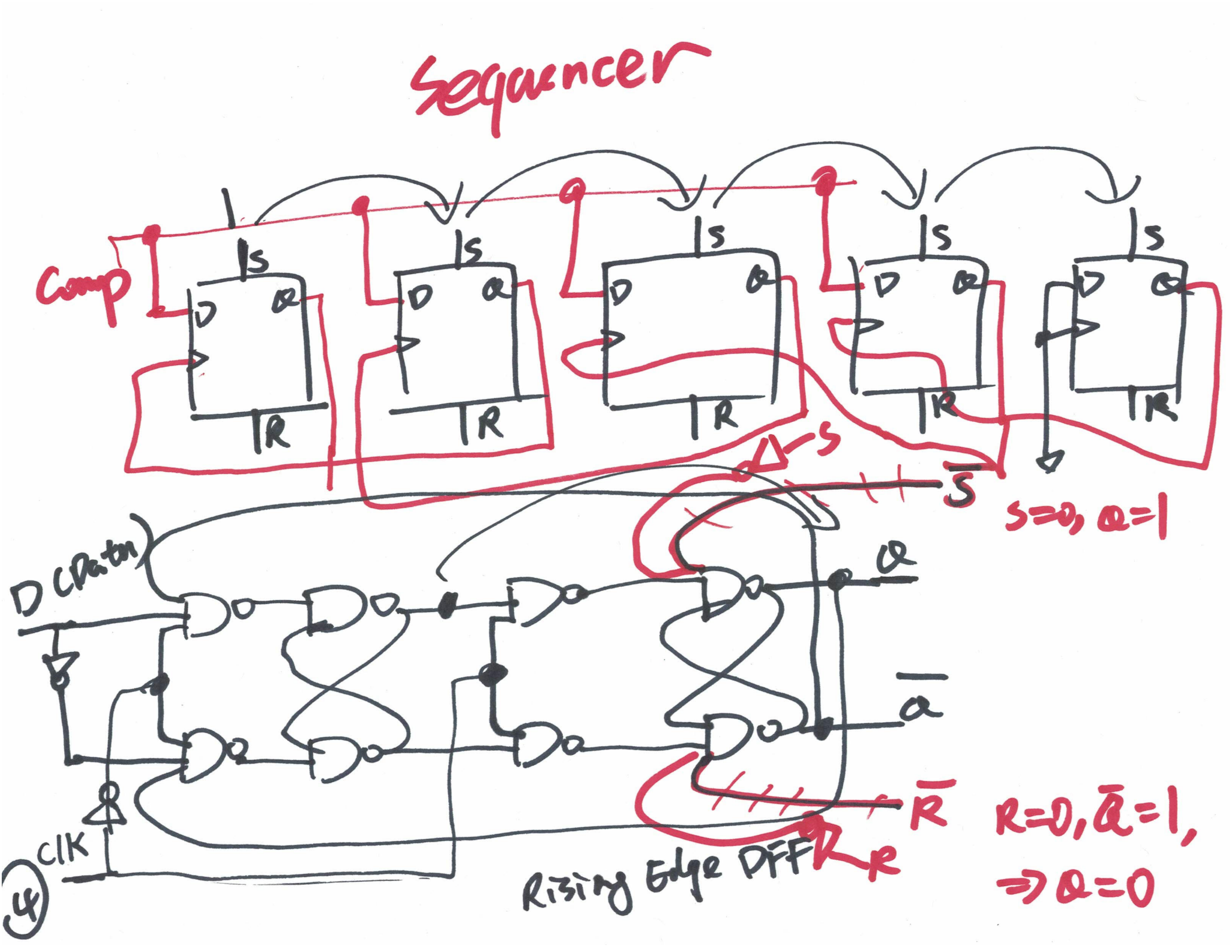
② the final ADC output is always smaller than or equal to the input voltage.

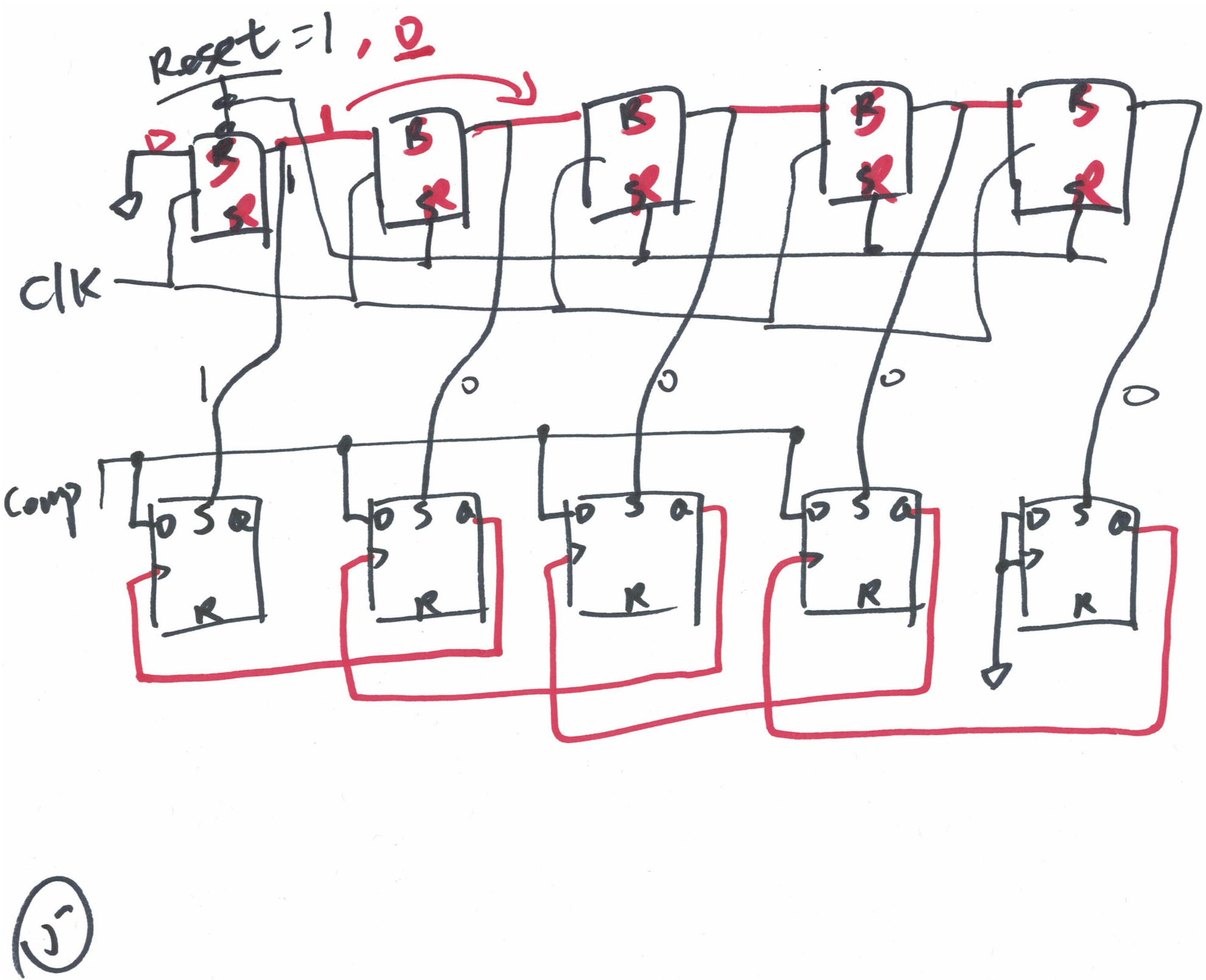
#	B_3	B_2	B_1	B_0	Comp
0	0	0	0	0	
1	1	0	0	0	A_3
2	A_3	1	0	0	A_2
3	A_3	A_2	1	0	A_1
4	A_3	A_2	A_1	1	A_0
5	A_3	A_2	A_1	A_0	



All possibilities of SAR ADC's output.

Sequencer


Comp
S
D
Q
R
$\bar{S}$
S=0, Q=1
D (Data)
Q
$\bar{Q}$
$\bar{R}$
R=0, $\bar{Q}$=1,
⇒ Q=0
CLK
Rising Edge DFF
(4)


Reset = 1, 0
clk
Comp
D S Q
R
1
0