HW5

① c5_models.txt → fabricatable (Pure-play foundry GlobalFoundries)

Vdd → 5V
V_{TH} → 800mV. 0.8V

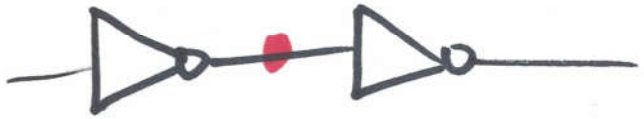
② models.txt = cmosedu_models.txt → Dr. Baker's CMOS Book

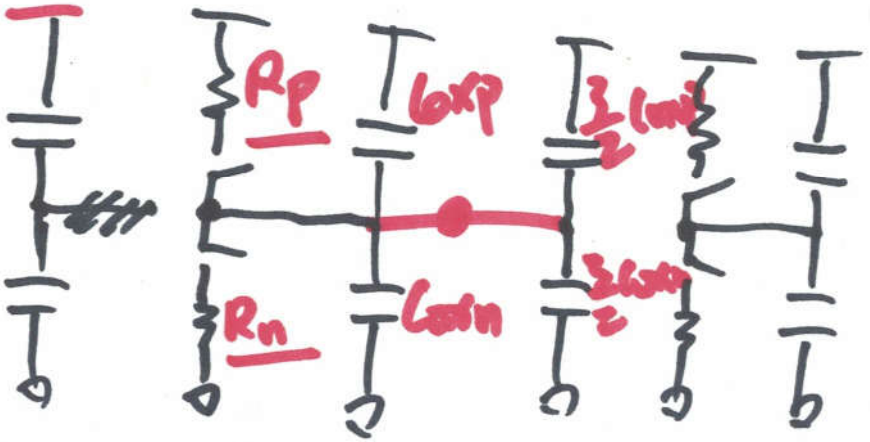
Not fabricatable.

N_1n	P_1n	→ Vdd → 5V, V_{TH}: 0.8V NMOS, 0.9V PMOS
N_50n	P_50n	→ Vdd → 1V, V_{TH}: 0.3V NMOS, — PMOS

1.(b)

3.

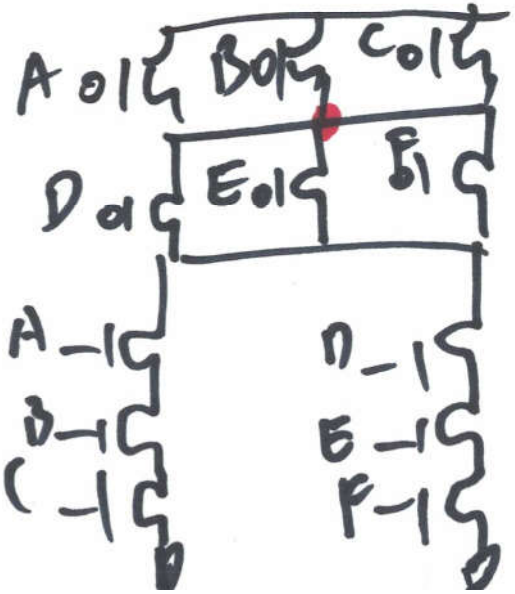


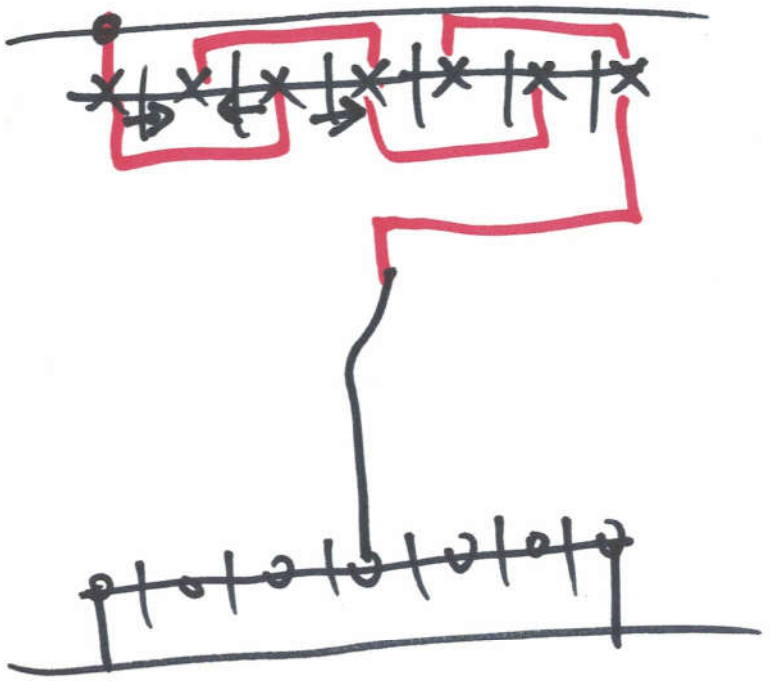


- 120 min
- 7 Problems
- close-book, close-notes, calculator is allowed
- May, 5, 9:45 - 11:45 am

① Stick diagrams (one line)

~~AB+~~ ABC + DEF





② CS layers (cross-sectional views)

③ Digital models. (ring oscillator. f_{osc}, TG, t_{PHL}, t_{PLH})

④ Clocked Circuits (clocked DFF, time delays)

~~⑨ SRAM, DRAM, flash~~

⑤ fabless / IDM / Pureplay (SRAM, DRAM, SDRAM.

Moore's law?

timeline of the technologies being commercialized.

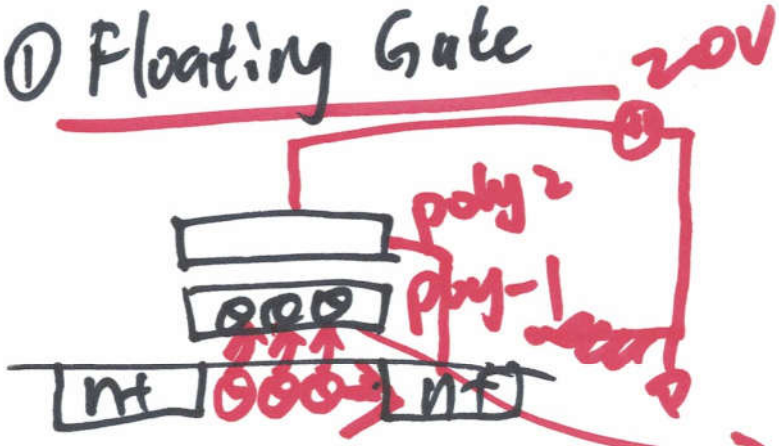
180nm / 65nm / 22nm / 10nm / and 5nm.

(6) SRAM / DRAM / flash

(1) BJTs. → similar to the HW assignments

Erasable ROM (EROM)

① Floating Gate



Channel Hot Electron (CHE)

cache V_{DS}

P-sub