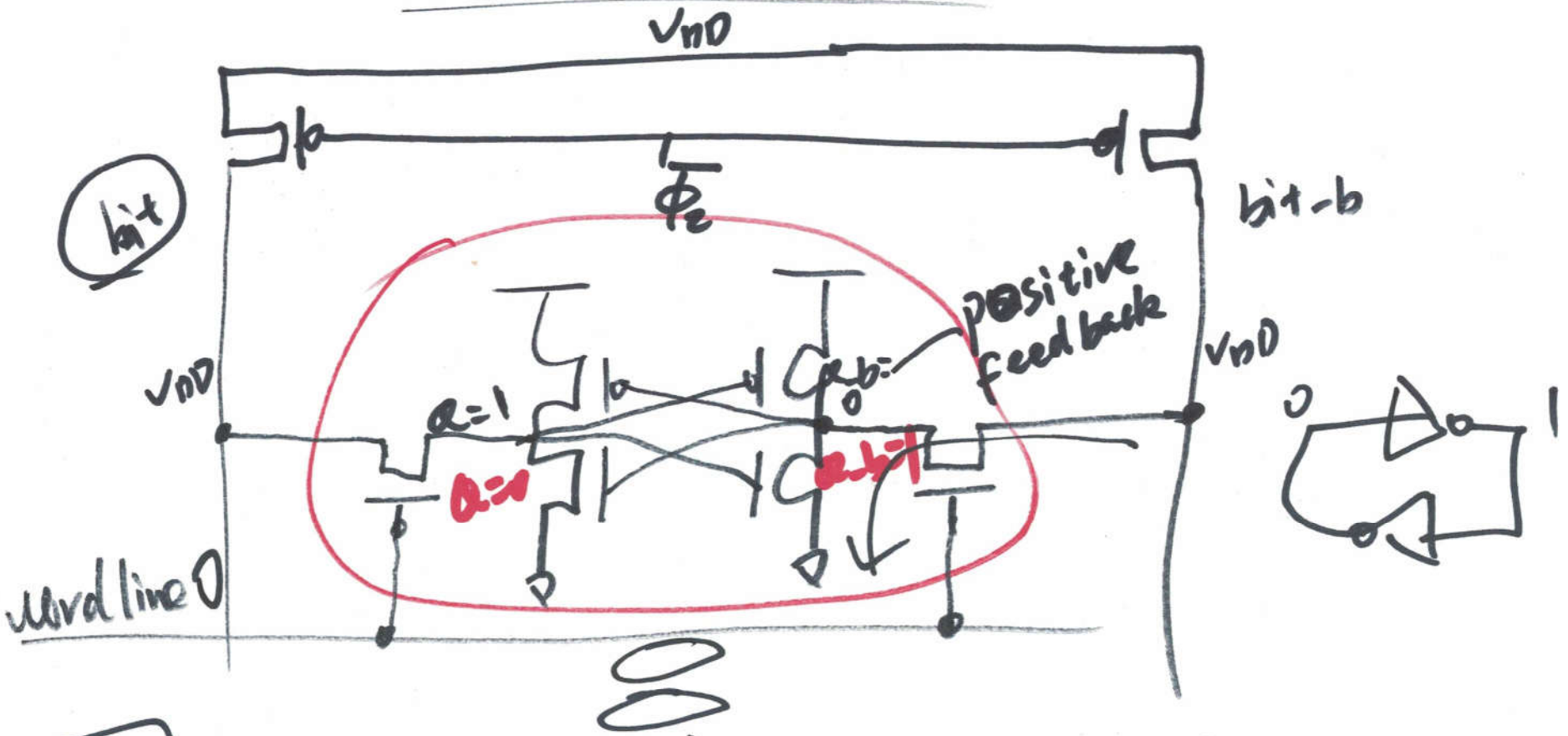
Static Random Access Memory

SRAM (6-Transistor)



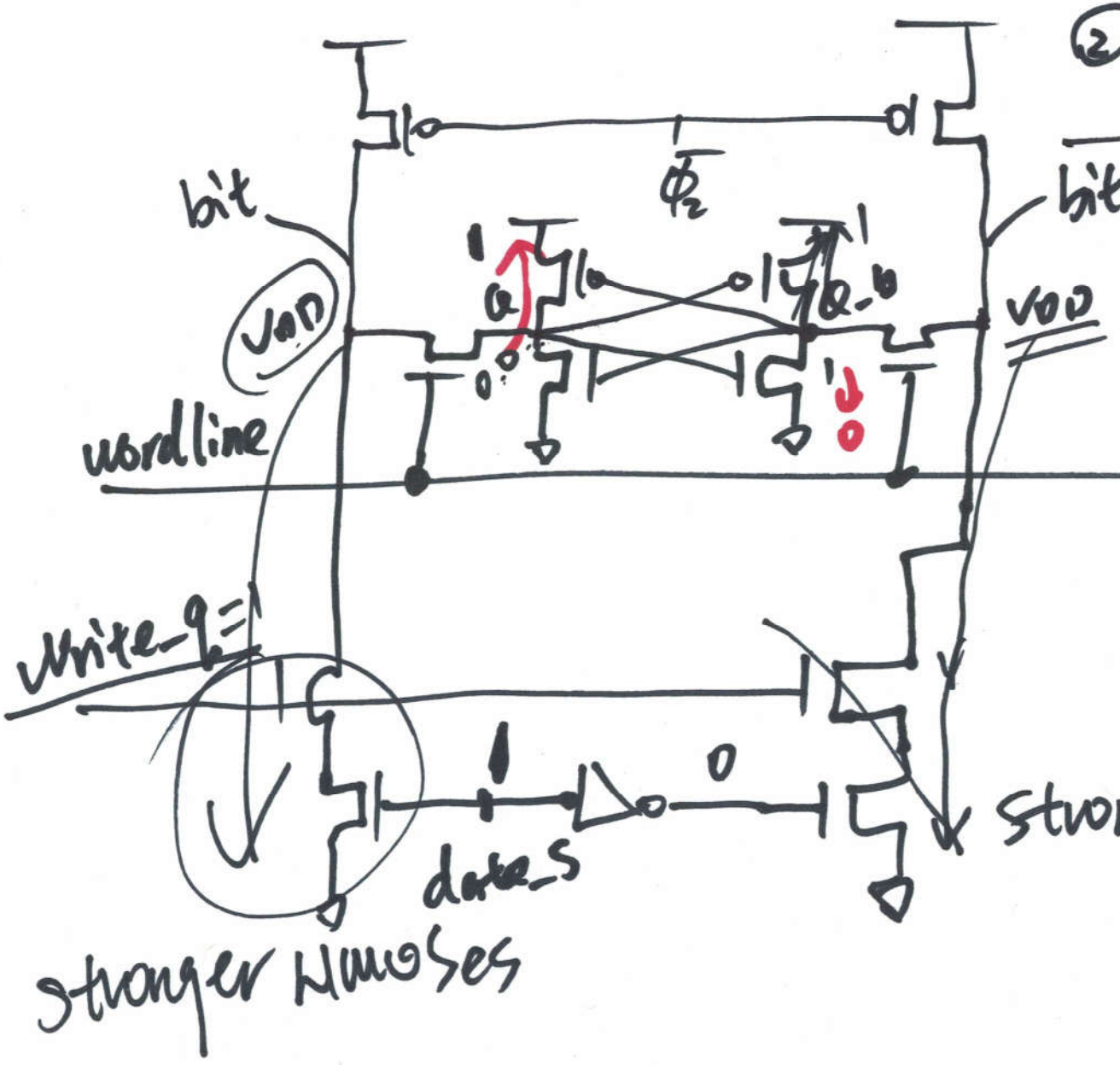
Read: ① Pre-charge the bit / bit_b lines to V_{DD}, then float them

② If Q=1, Q_b=0, read the bit line, V_{DD}. bit_b will be discharged to GND

Fire the wordline

③ If Q=0, Q_b=1, fire wordline, bit line will be discharged to GND

write 0 operation



write 1 to Q

① Pre-charge bit/bit_b to Vdd.

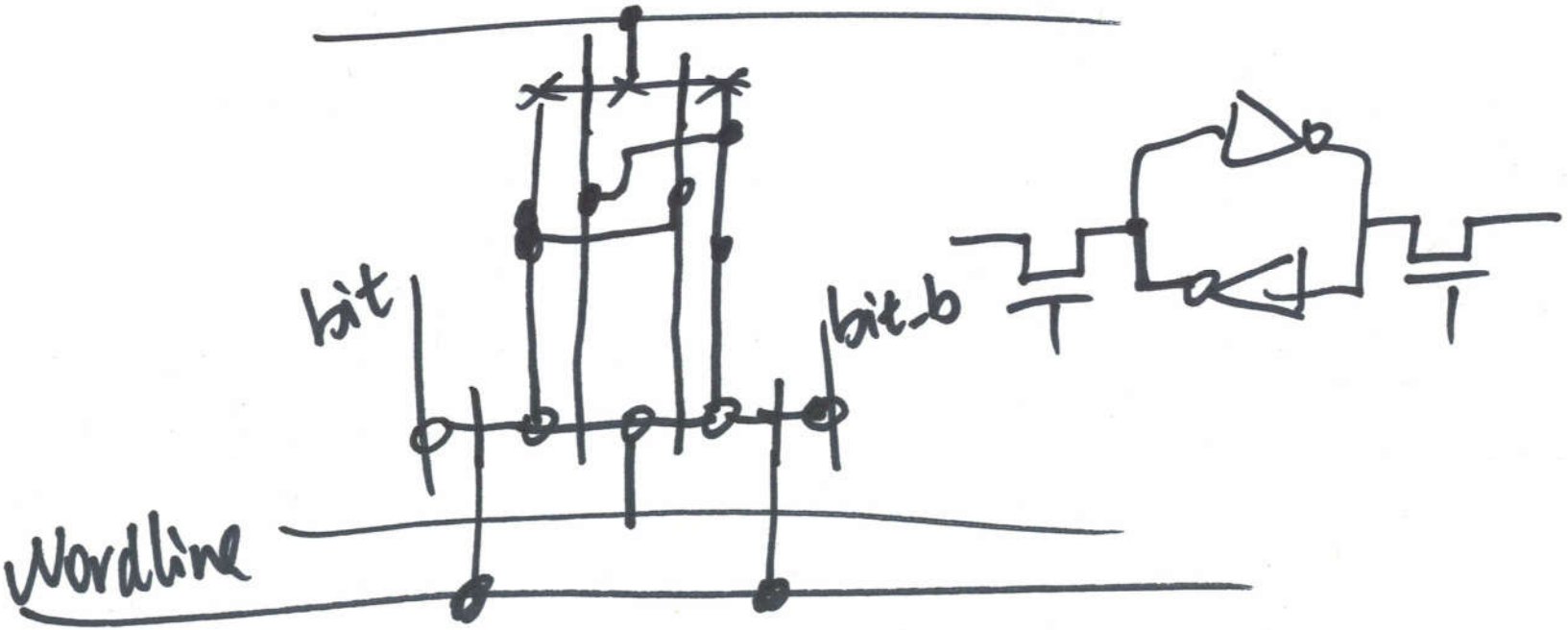
② ~~data_s~~ data_s = 0
write_q = 1

write 0 to Q

① Pre-charge bit/bit_b to vdd.

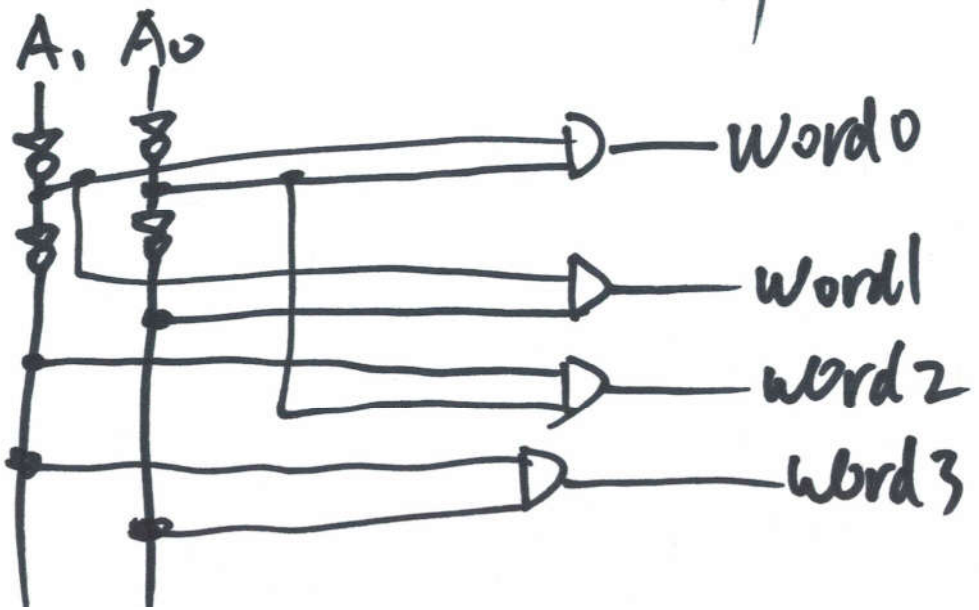
② data_s = 1
write_q = 1

Layout of 6-transistor SRAM cell

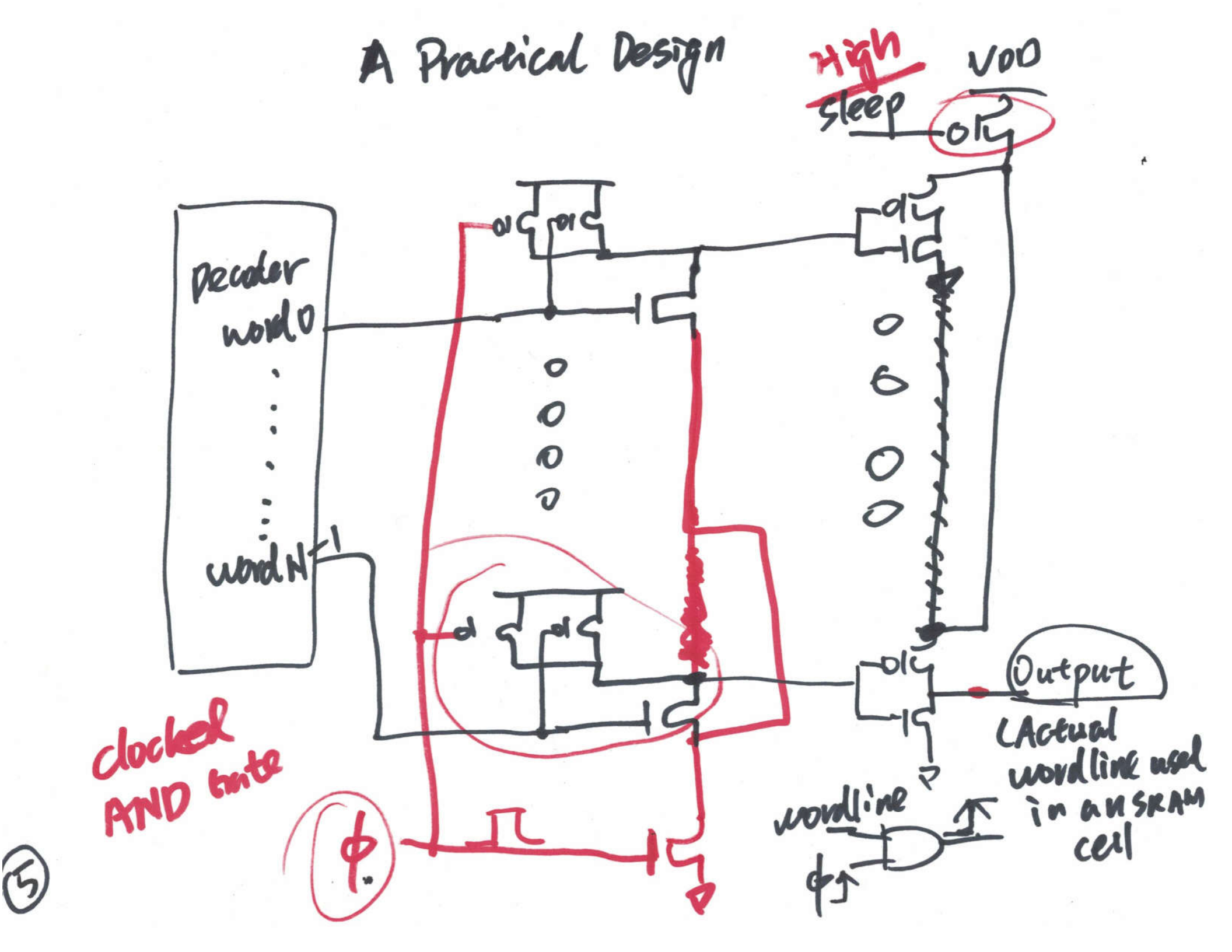


Row circuitry (Decoders)

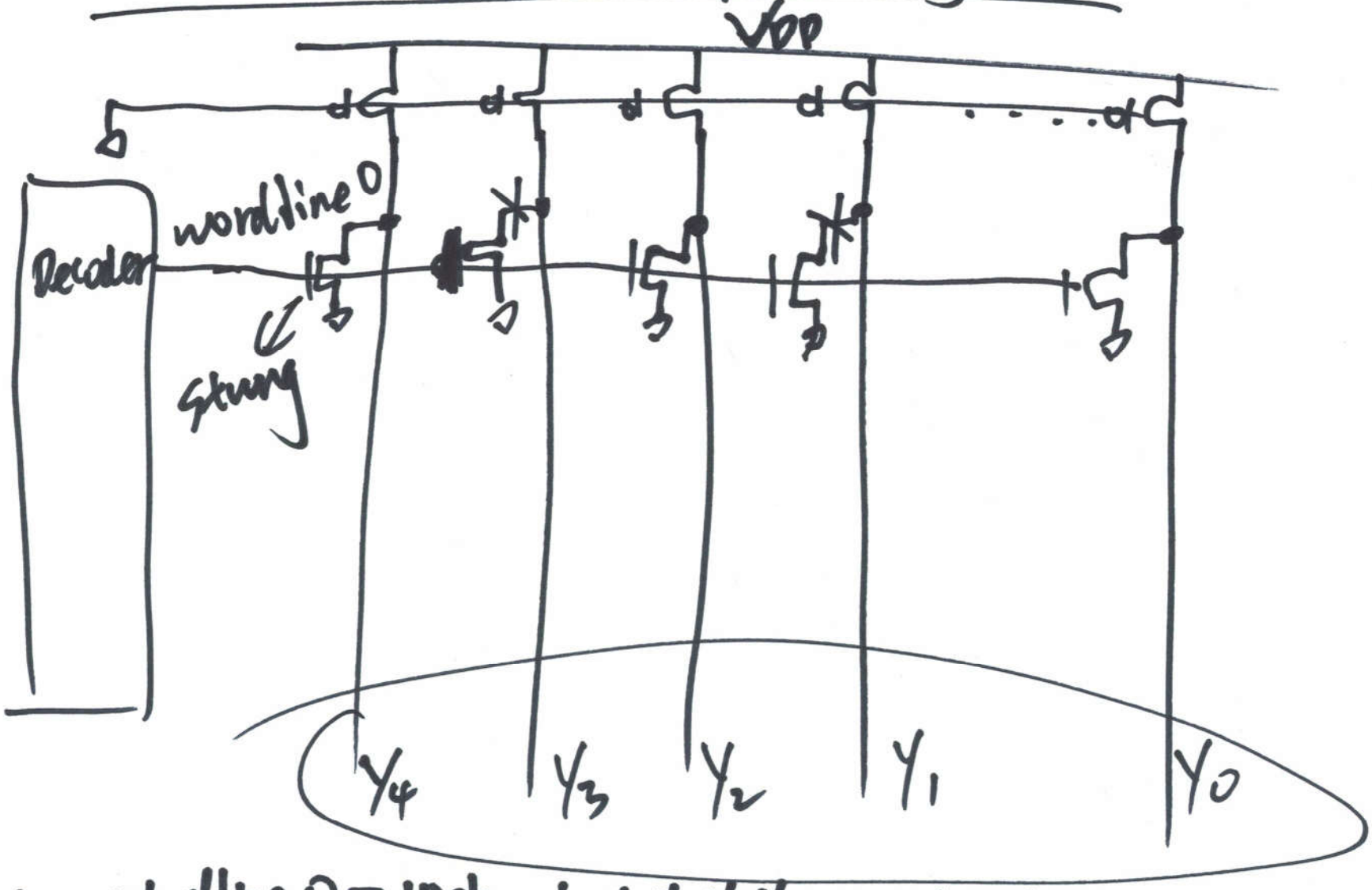
A_1	A_0	word 0	word 1	word 2	word 3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



A Practical Design



ROM: Read Only Memory (non-volatile)



when wordline 0 is High: $Y_4 Y_3 Y_2 Y_1 Y_0 = 0\,1\,0\,1\,0$

(6)