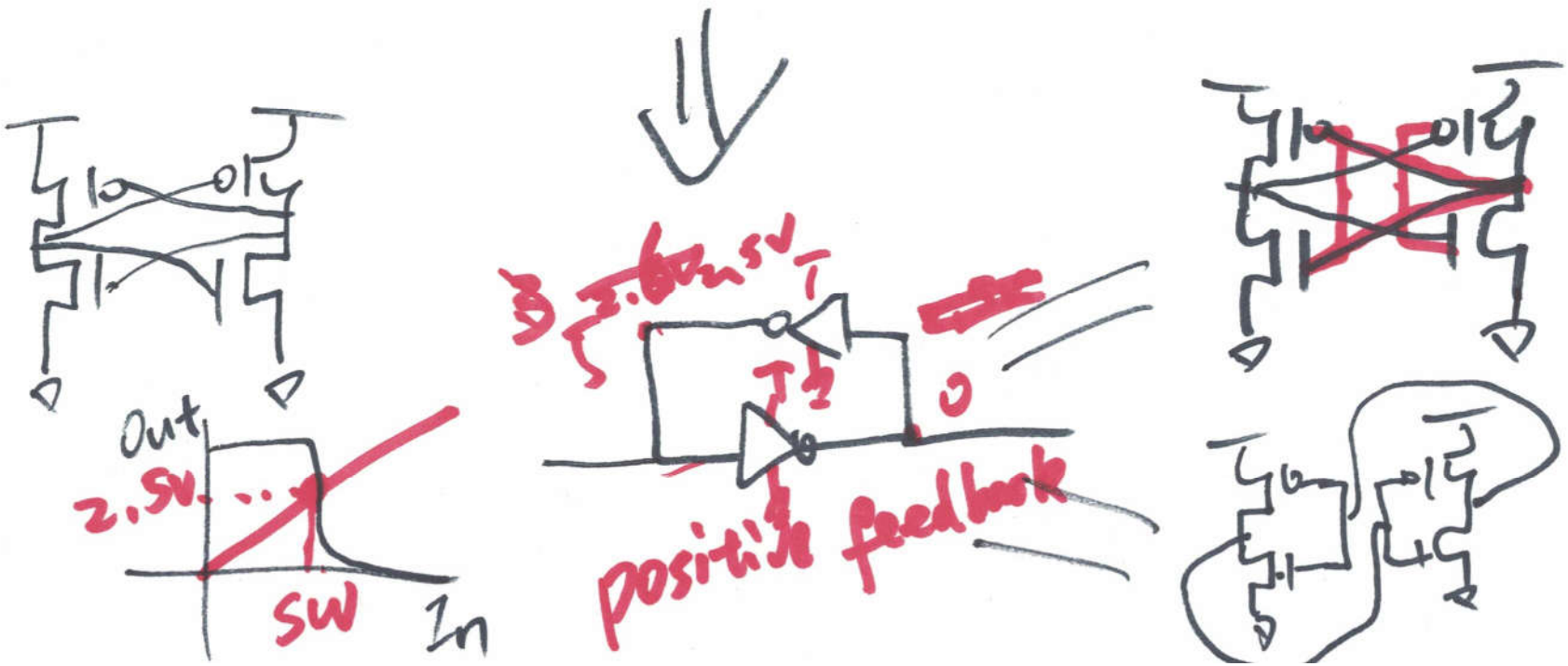
Clocked Circuit

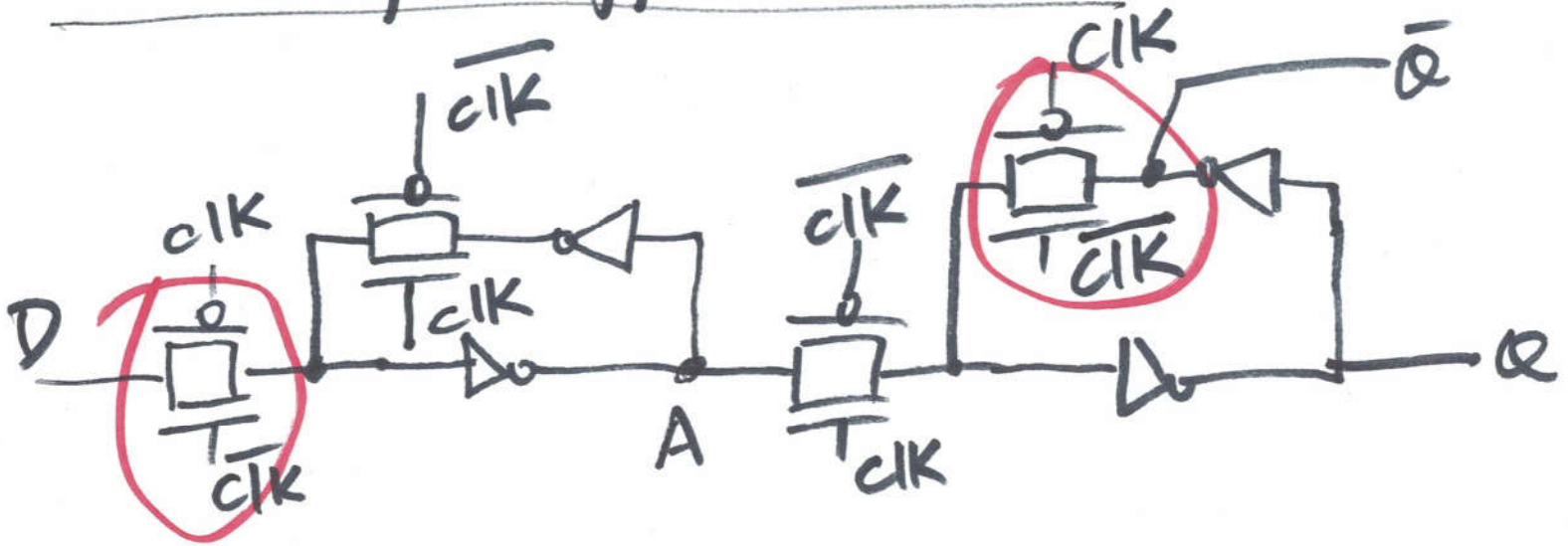
① A level sensitive latch (level-~~triggered~~ FF)

Figure 13.21 P386

Latch, stores the signal



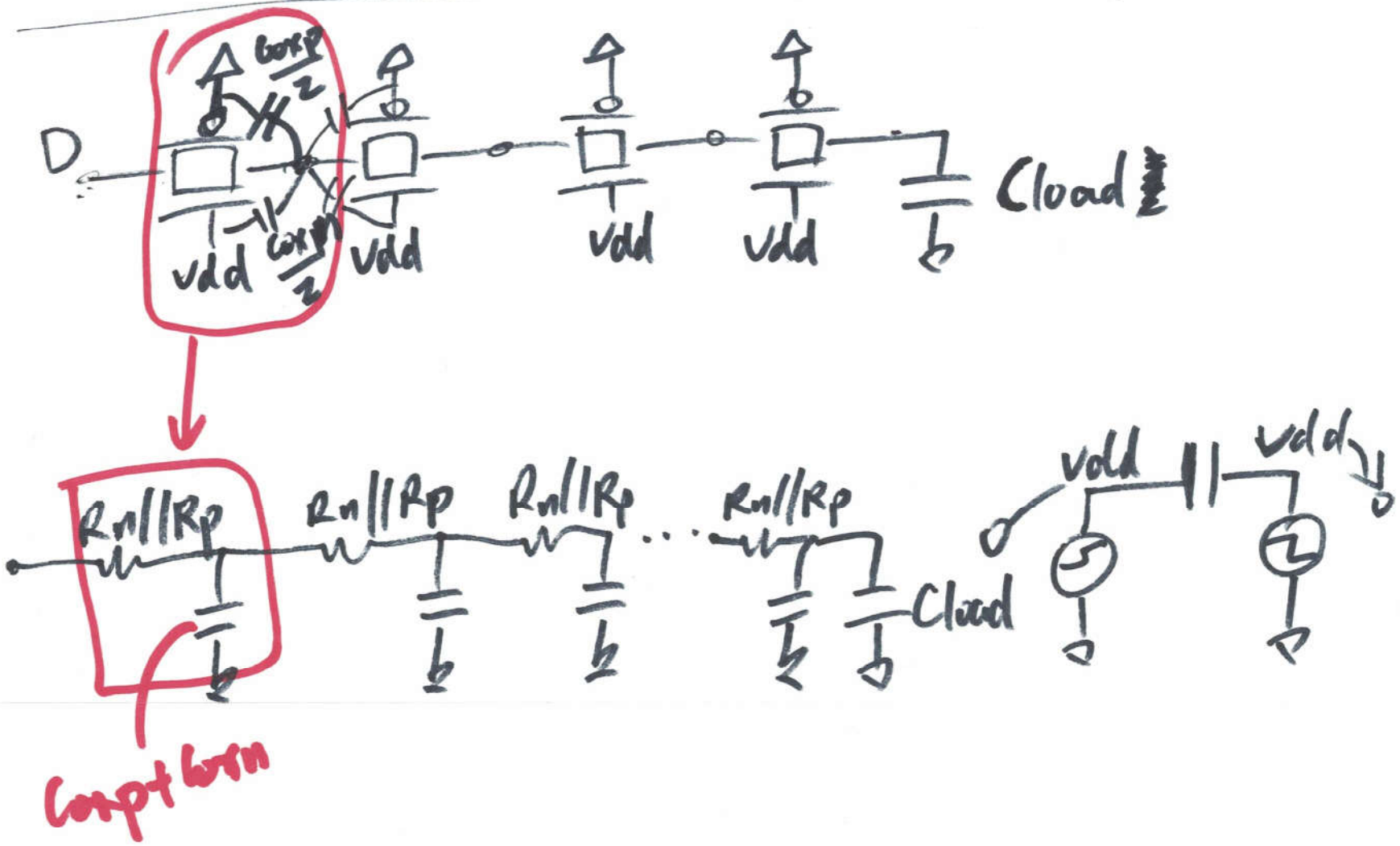
② An edge triggered DFF



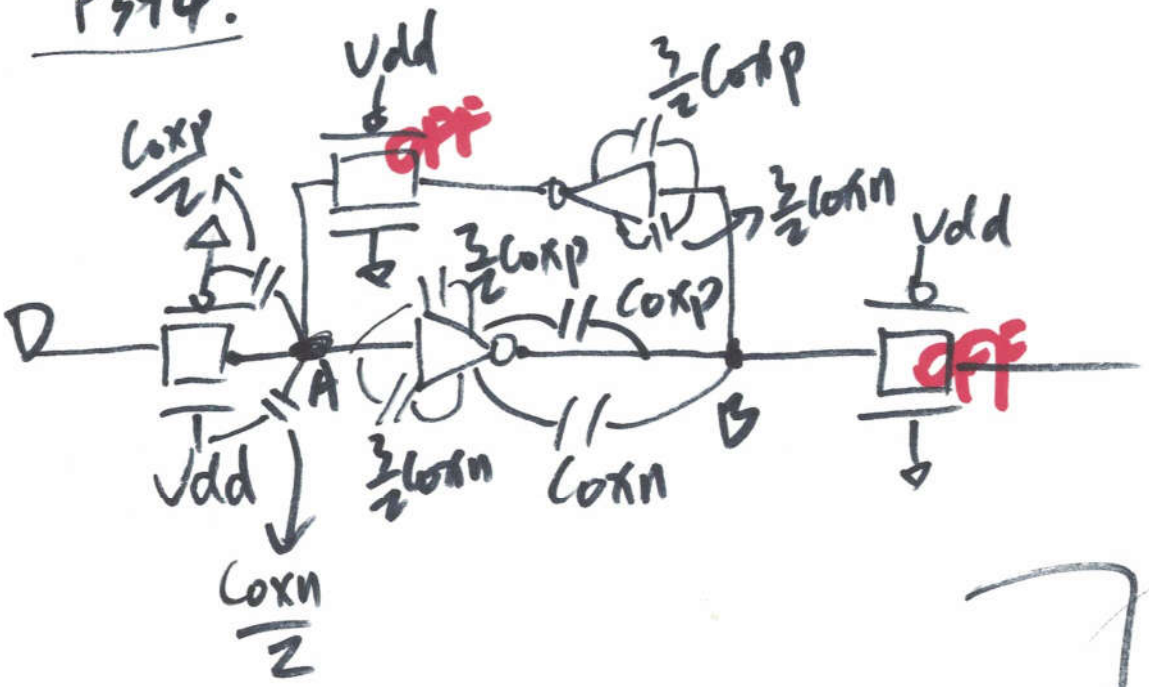
A is sent to Q (rising edge triggered)

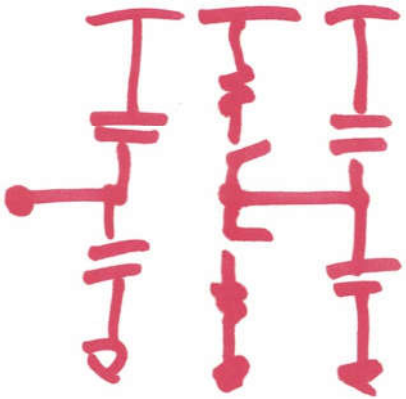
D is sent to A (Data is being sampled)

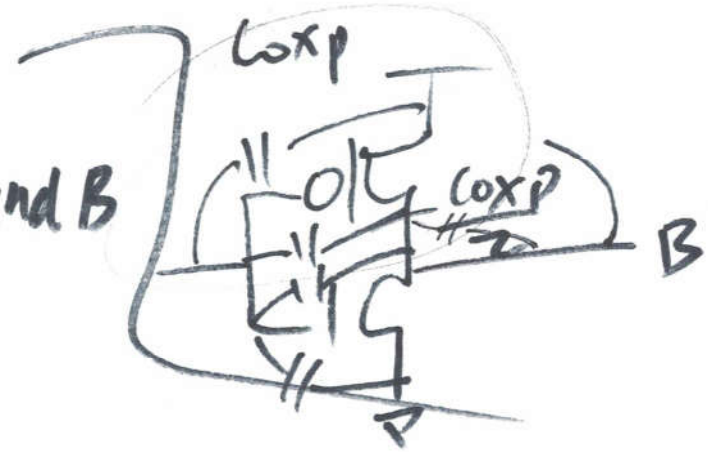
③ RC Digital Model for TGs



P394.







Estimate the Delay from D to A, and B

NMOS: $R_n = 3.4K$, $C_{oxn} = 0.625f$

PMOS: $R_p = 3.4K$, $C_{oxp} = 1.25f$

$$C_A = \frac{C_{oxn}}{2} + \frac{C_{oxp}}{2} + \frac{3}{2}(C_{oxn} + C_{oxp}) = 2(C_{oxn} + C_{oxp})$$

$$= 2(1.875f) = 3.75fF$$

$$C_B = C_{oxn} + C_{oxp} + \frac{3}{2}(C_{oxn} + C_{oxp})$$

$$= \frac{5}{2}(C_{oxn} + C_{oxp}) = 4.7\,fF$$

Delay from D to A: (always look at the output)

$$t_{pHL} = t_{pLH} = 0.7\,(R_n \| R_p) \cdot C_A$$

$$= 4.5\,ps$$

p 10^{-12}

f 10^{-15}

Delay from A to B:

$$t_{pLH\,B} = 0.7 \cdot R_p \cdot C_B = 0.7 \cdot 3.4K \cdot 4.7fF$$

$$= 11.2\,ps$$

$$t_{pHL\,B} = 0.7\,R_n \cdot C_B = 0.7 \cdot 3.4K \cdot 4.7fF$$

$$= 11.2\,ps$$

The Propagation delay from D to B is:

$t_{PHL} = 4.5ps + 11.2ps = 15.7ps$

$t_{PLH} = 4.5ps + 11.2ps = 15.7ps$

Memory Circuits

	SRAM	DRAM	SDRAM	ROM	Flash
volatile	x	x	x		

RAM: Random Access Memory

DRAM: Dynamic RAM

SRAM: Static RAM

SDRAM: Synchronous DRAM

SRAM	DRAM
less power	—
faster	—
insensitive to noise	—
used inside the CPU chip for cache	off-chip (card)
20-40ns	60-100ns
6-transistor circuit	transistor capacitor

Double Data Rate SDRAM

DDR → 2000

DDR2 → 2003

DDR3 → 2007

DDR4 → 2014

DDR5 → 2020

16GB DDR4 SDRAM $60.

Main players make SDRAMs:

Micron, Samsung, Hynix

Boise, ID

(B)