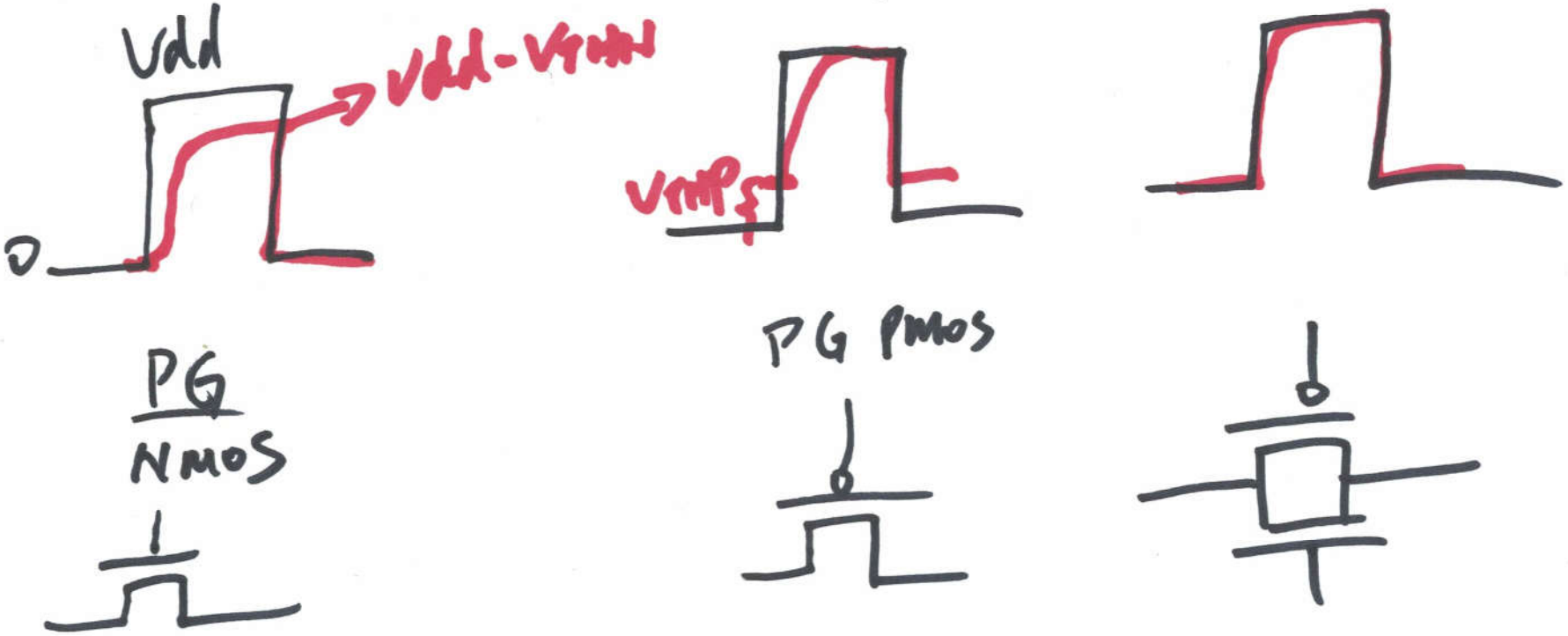
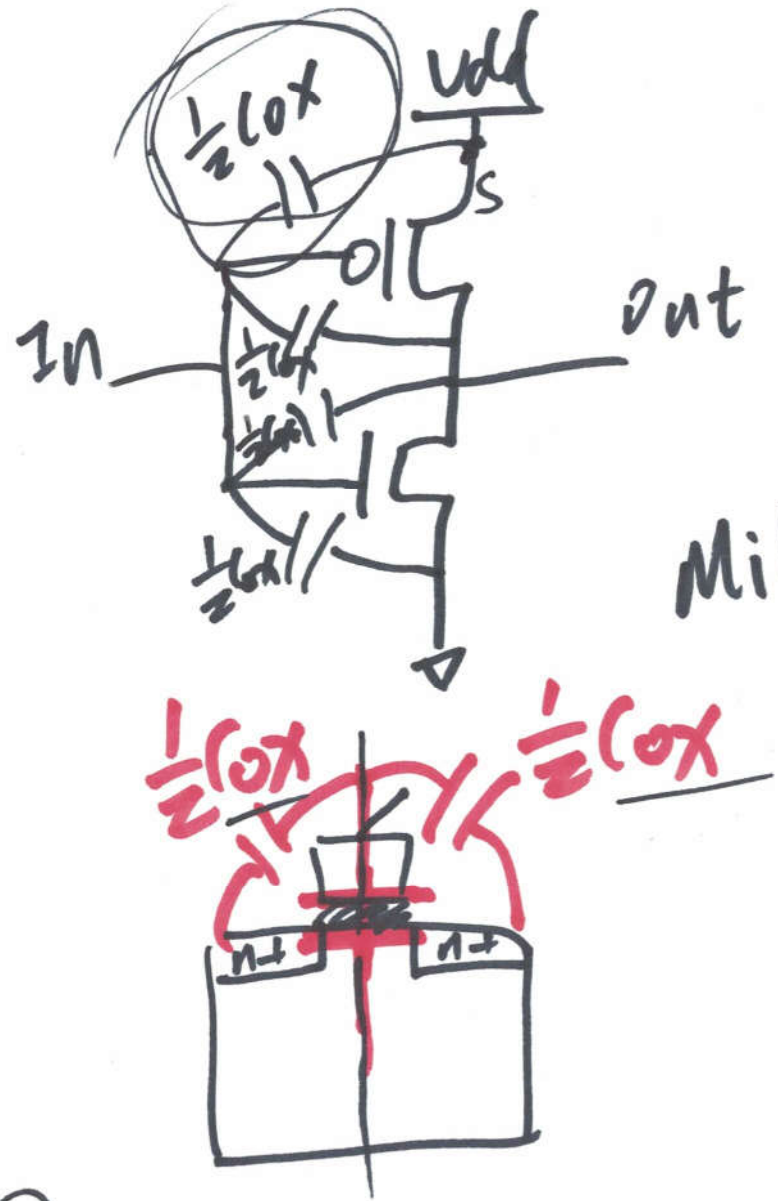
GDS II

① Models for Digital Design.



②

② Inverter Switching Characteristics



Miller Effect

Due to the Miller Effect

$$C_{inp} = \frac{1}{2}C_{ox_2} + C_{ox_2}$$

$$= \frac{3}{2}C_{ox_2}$$

$$C_{inn} = \frac{1}{2}C_{ox_1} + C_{ox_1}$$

$$= \frac{3}{2}C_{ox_1}$$

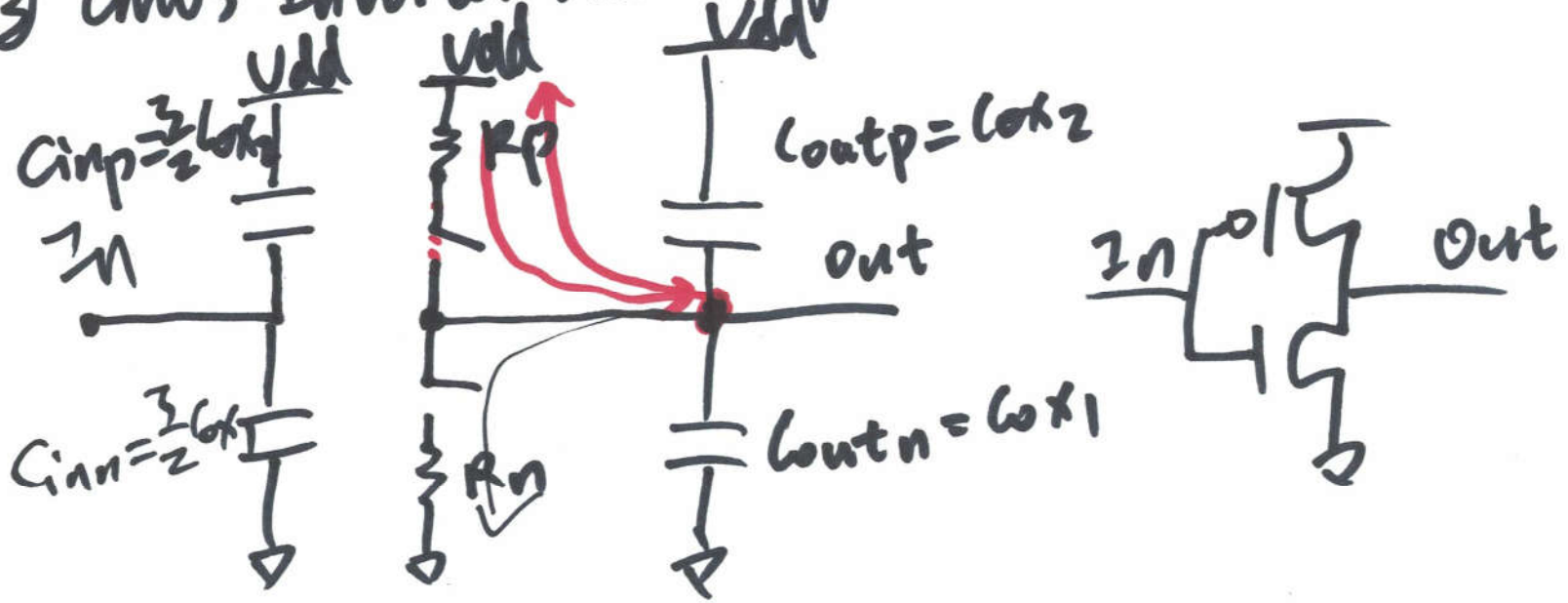
$$C_{in} = C_{inn} + C_{inp}$$

$$= \frac{3}{2}(C_{ox_1} + C_{ox_2})$$

$C_{outp} = C_{ox_2}$, $C_{outn} = C_{ox_1}$

$C_{out} = C_{outn} + C_{outp} = C_{ox_1} + C_{ox_2}$

③ CMOS Inverter Switching Model



④ Intrinsic Propagation Delay of the Inverter

$t_{pLH} = 0.7 RC = 0.7 R_p C_{tot}$

$t_{pHL} = 0.7 RC = 0.7 R_n C_{tot}$

Example:

Estimate the intrinsic propagation delay of the following inverter P320, Table 10.2

NMOS: 10/1 0.5um/50nm. $K_n = 3.4k$

$C_{oxn} = 0.625fF$

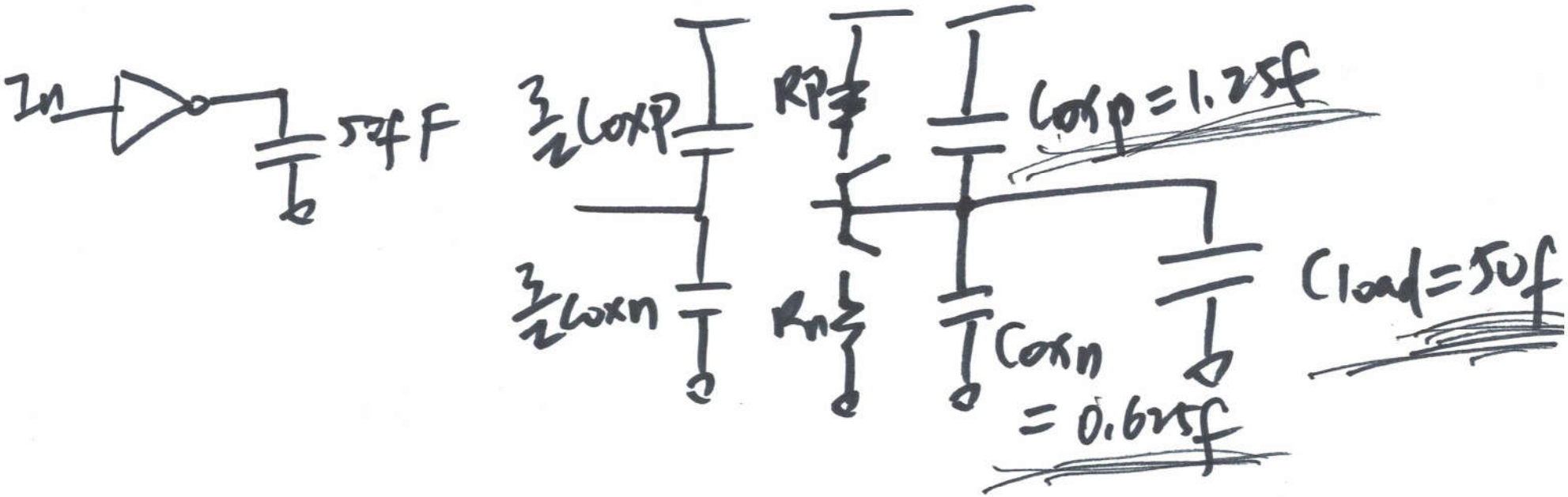
PMOS: 20/1, 1um/50nm. $R_p = 3.4K$.

$C_{oxp} = 1.25fF$

$$t_{plit} = t_{pHL} = 0.7 \times 3.4K \times (0.625f + 1.25f) \quad 10^{-15}$$

$$= 4.5 ps.$$

If the inverter is used to drive a 50fF load, what are the intrinsic propagation delays?



$$t_{pHL} = t_{pLH} = 0.7 R C_{tot}$$

$$= 0.7 R \ (50fF)$$