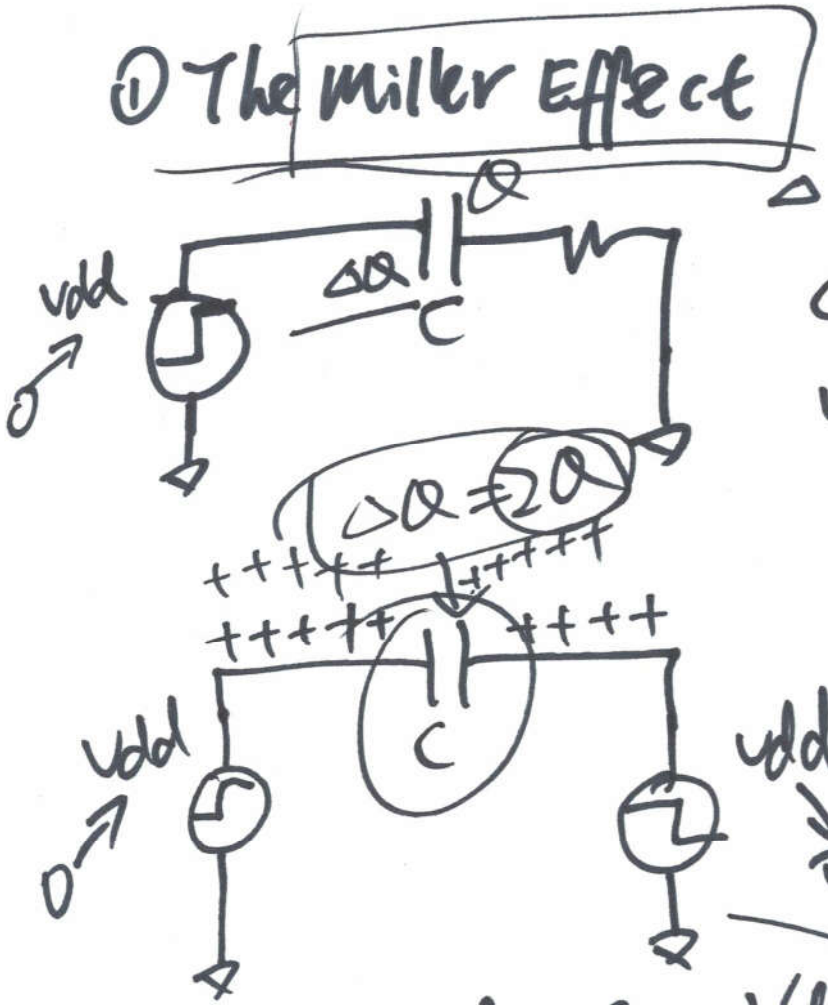
Models for Digital Design

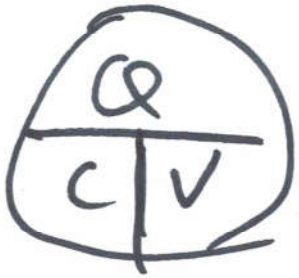
① The Miller Effect

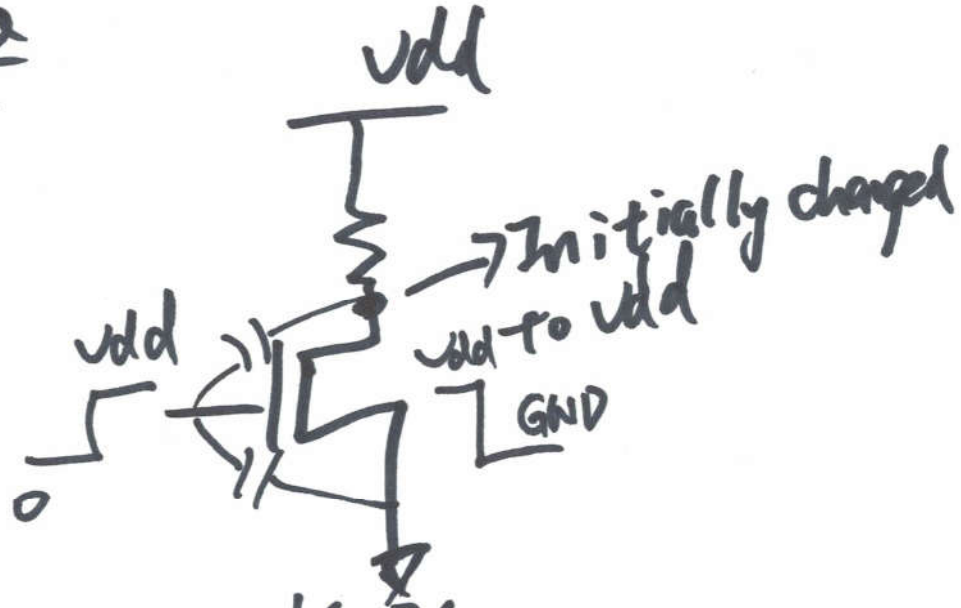


$\Delta Q = C \cdot V$

$C = \frac{\Delta Q}{V}$

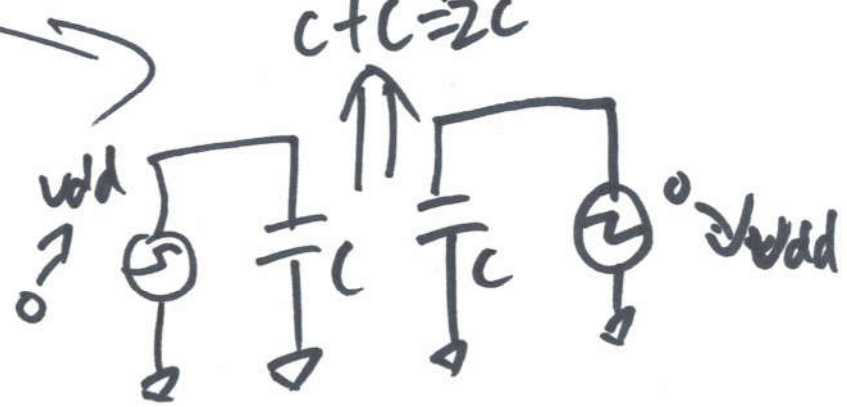
$V = \frac{\Delta Q}{C}$

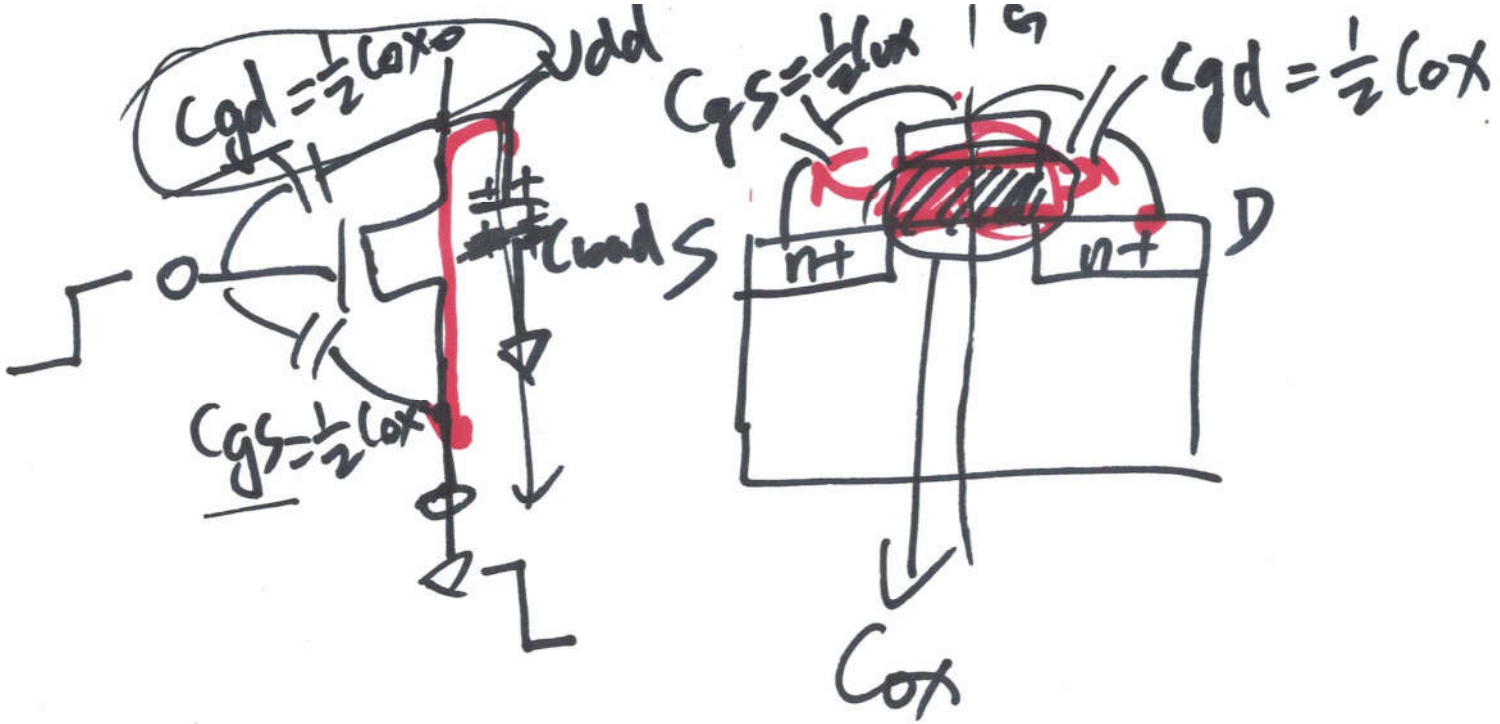




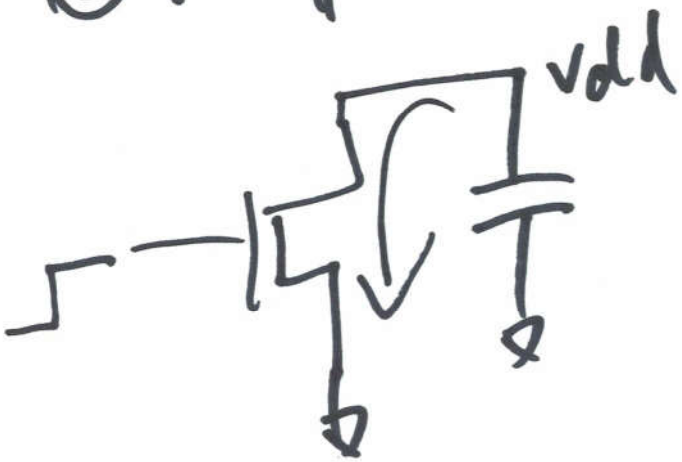
$2Q = C_{eff} \cdot Vdd$

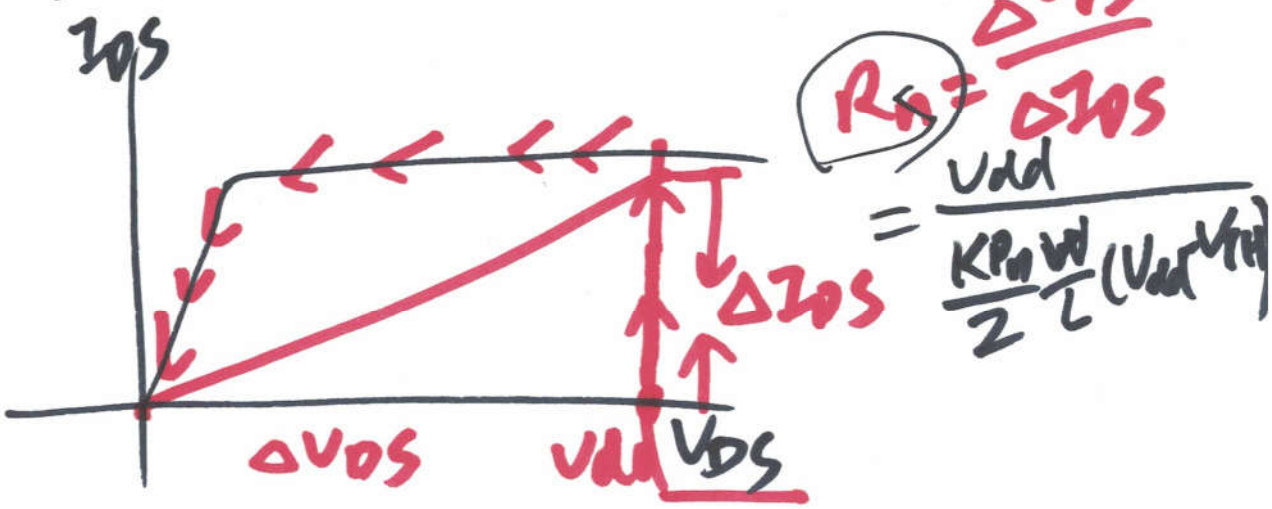
$C_{eff} = \frac{2Q}{Vdd} = 2C$





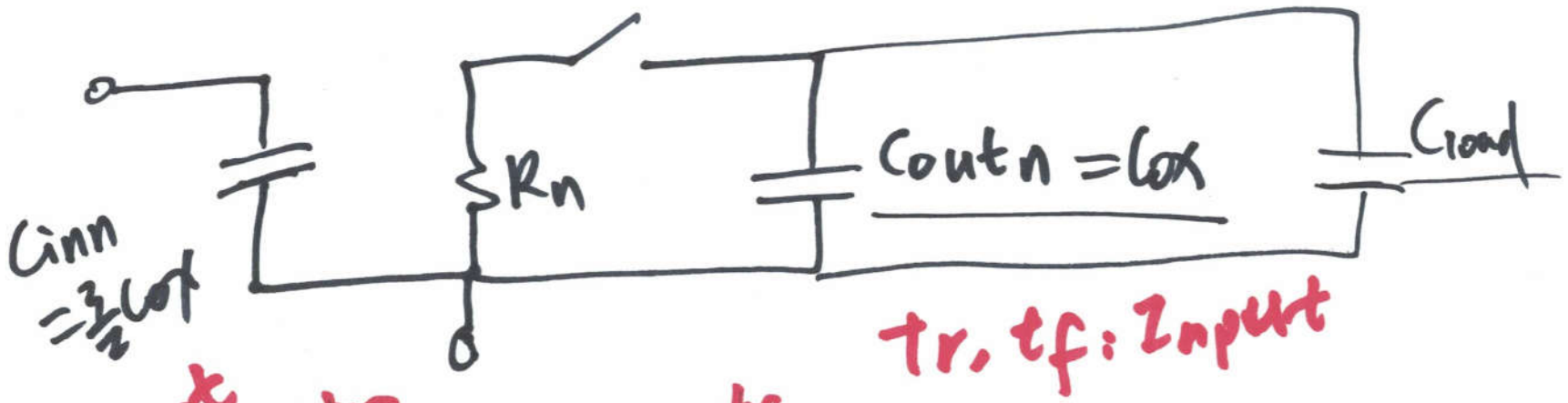
② The Effective switching Resistance of cmos R_n, R_p



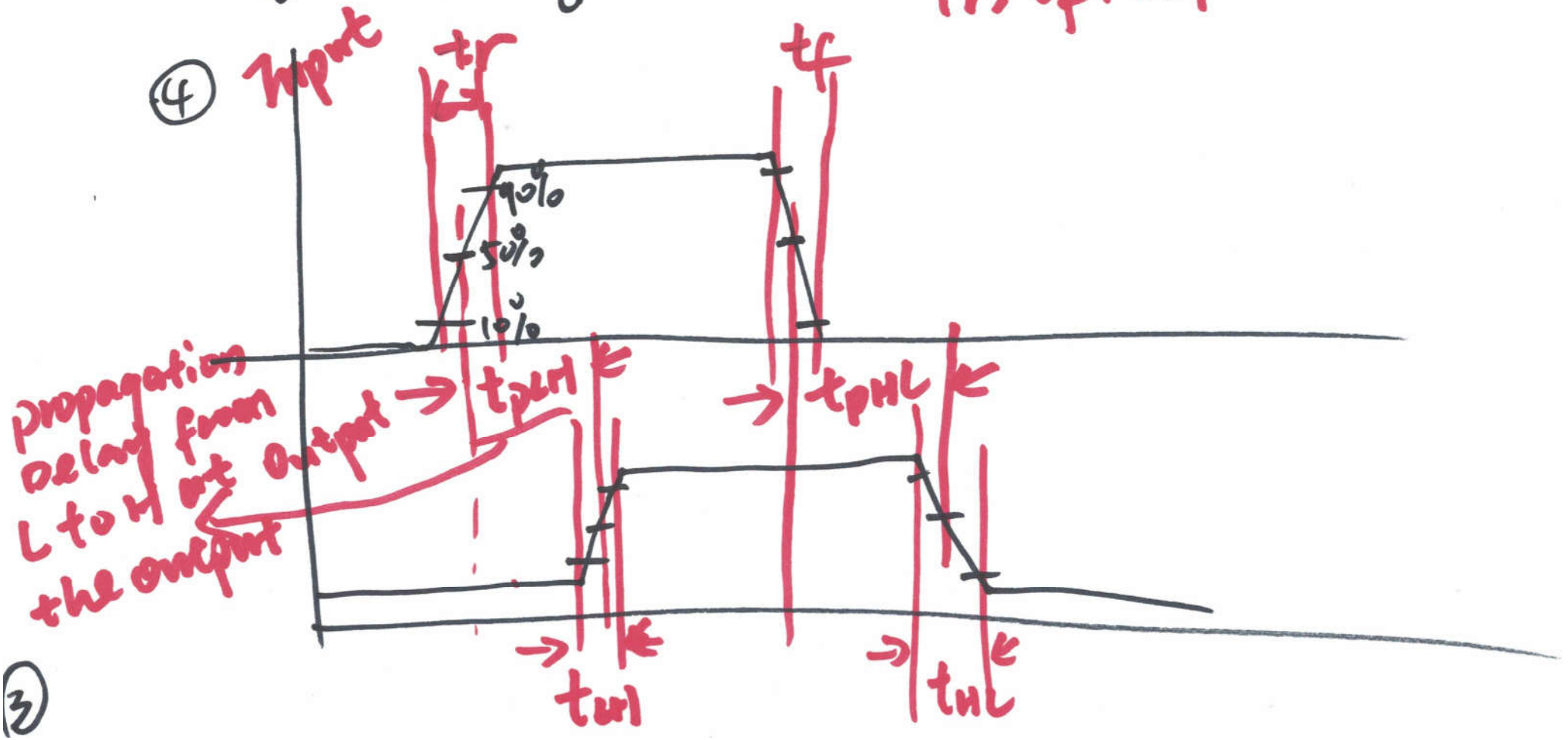


$$R_n = \frac{\Delta V_{DS}}{\Delta I_{DS}} = \frac{V_{dd}}{\frac{K P_n W}{2 L}(V_{dd} - V_{th})}$$

③ The complete resistive/capacitive switching MOSFET model:



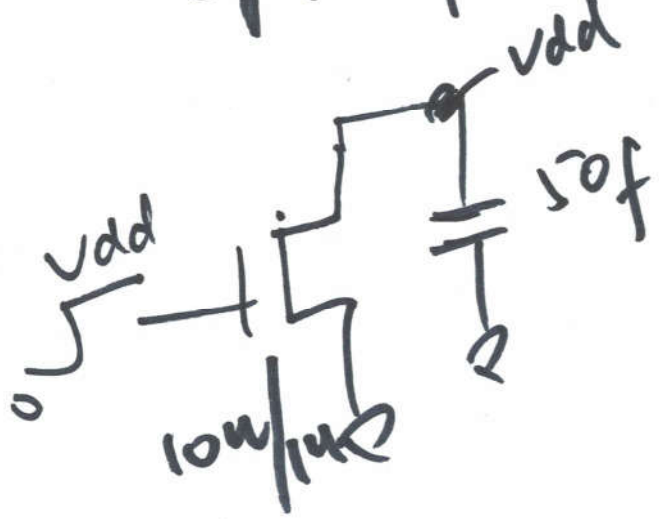
④



t_{PHL} or t_{PLH} = 0.7RC

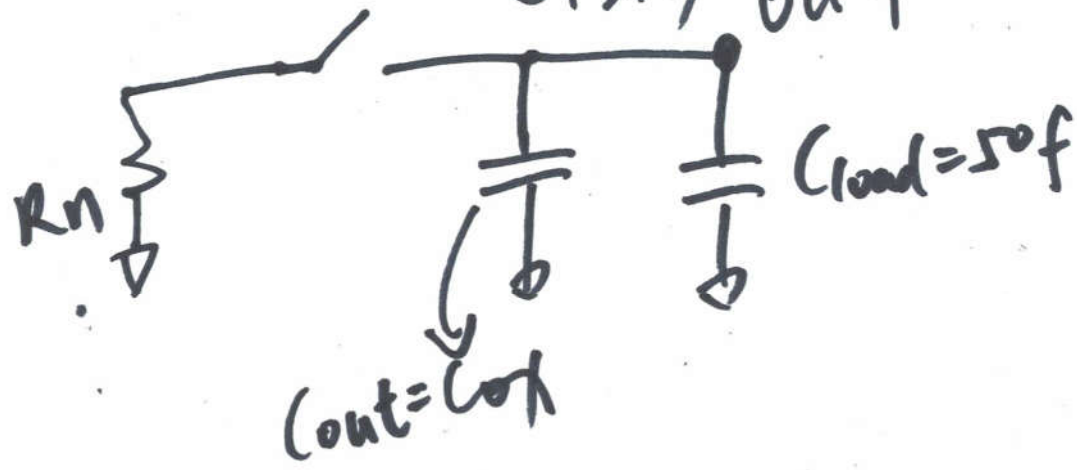
t_{HL} or t_{LH} = 2.2RC (P50 of the CMOS Book)

Example: Estimate the fall and delay times (output) of the following circuit: (P320)



	Size	$R_{n,p}$	Cgate,p
NMOS	10u/1u	1.5K	17.5f
PMOS	30u/1u	1.5K	52.5f

(P317)



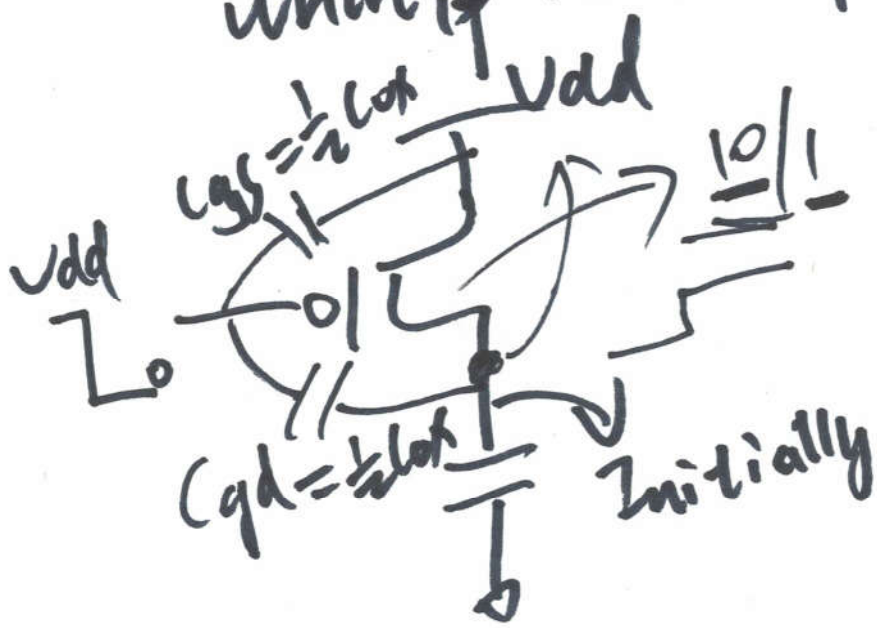
$t_{HL} = 2.2RC = 2.2 \times 1.5K \cdot (17.5f + 50f) = 220ps$

$t_{pHL} = 0.7RC = 0.7 \times 1.5K \times (17.5f + 50f) = 70ps$

what if it is a pmos?

$R_p = 1.5K \times 3 = 4.5K$

$C_{oxp} = \frac{52.5f}{3} = 17.5f$



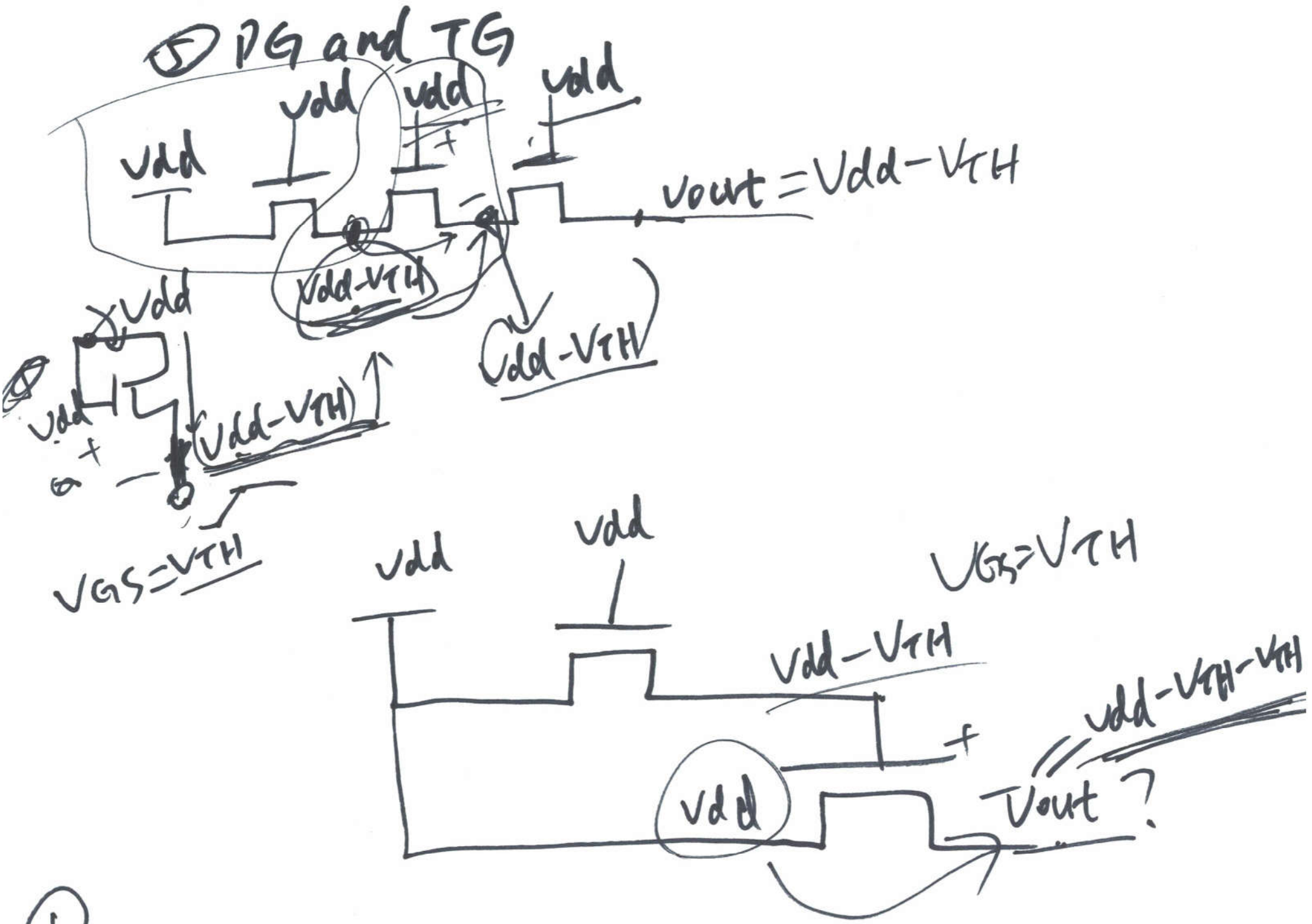
$t_{LH} = 2.2RC$

$= 2.2 \times 4.5K \times (17.5f + 50f)$

$= 660ps$

$t_{pLH} = 0.7RC = 0.7 \times 4.5K \times (17.5f + 50f)$

$= 210ps$


5 PG and TG
Vdd
Vdd
Vdd
Vdd
Vout = Vdd - VTH
Vdd - VTH
Vdd - VTH
Vdd
Vdd
Vdd - VTH
VGS = VTH
Vdd
Vdd
VGS = VTH
Vdd - VTH
Vdd - VTH - VTH
Vdd
Vout ?
6