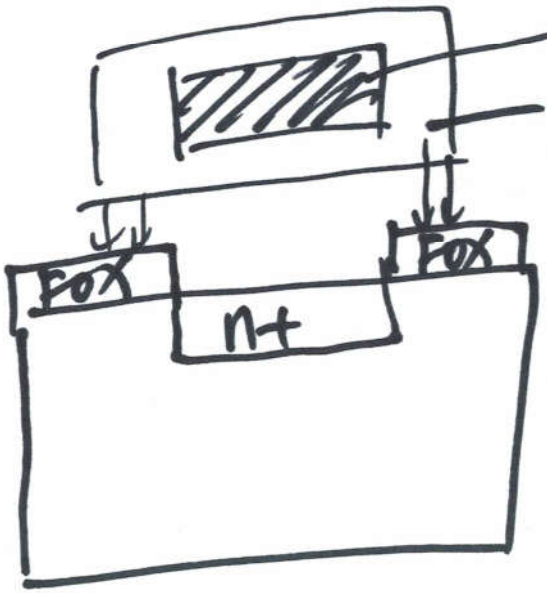
More CS Layers

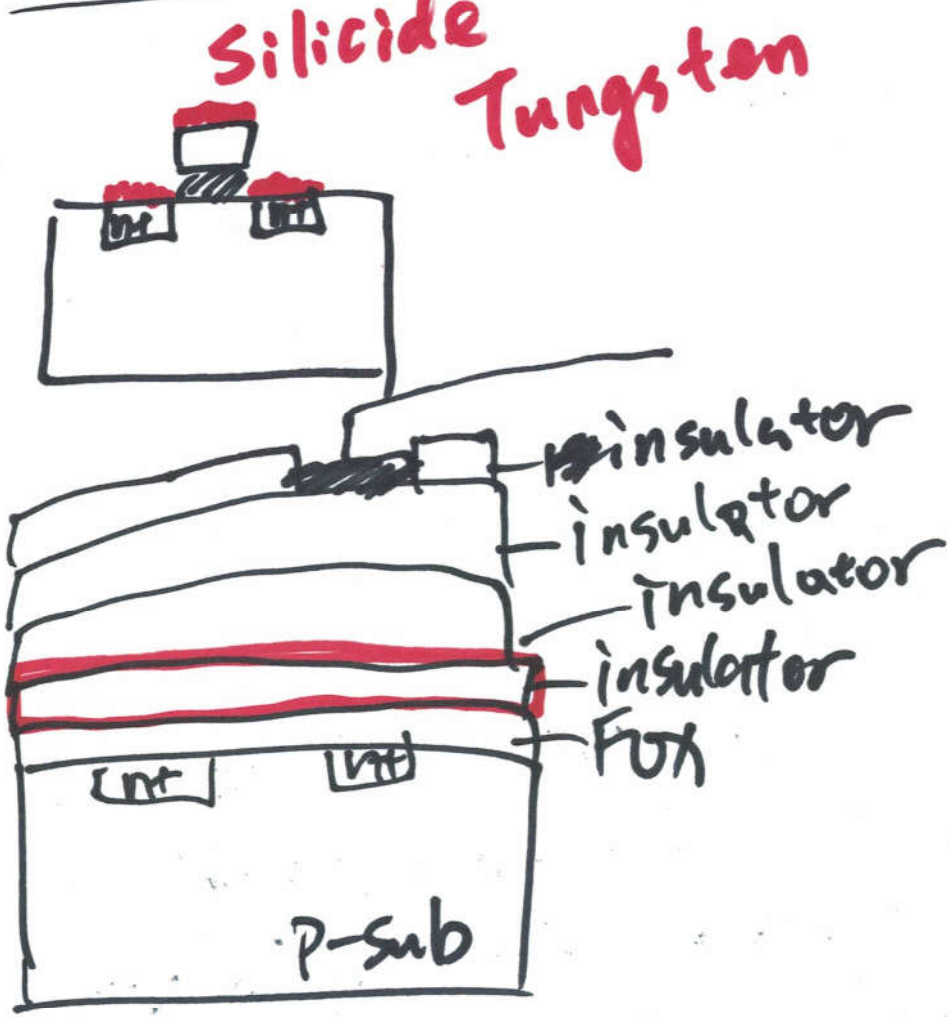


~~reduce~~
minimize
the misalignment

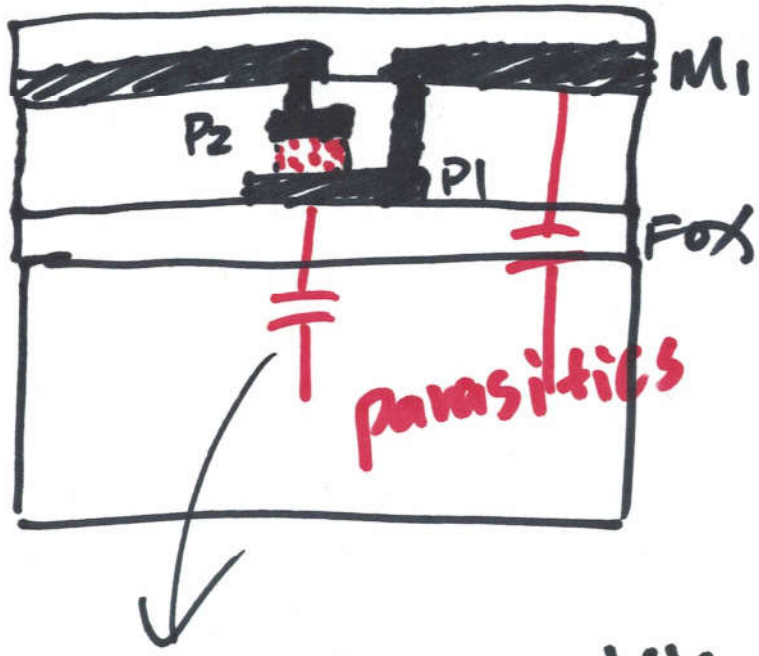
poly-silicon gate is self-aligned

Deposit poly first

poly used as a resistor



	Ω/square
poly	200 Ω/square
metal	0.1 Ω/square



bottom plate parasitic is larger than the metal1-sub parasitic

C_{ox}

$$C_{ox} = \frac{\varepsilon_0 \cdot \varepsilon_r}{t_{ox}} \cdot A$$

epsilon

ε_0: the permitivity of vaccumum.

ε_r: the permitivity of the oxide

$\varepsilon_0 = 8.85 \times 10^{-18}$ F/um

$= 8.85$ aF/um

atto: 10^{-18}

Example: $C_{ox}' = 25\,fF/\mu m^2$

In a 50 nm, poly-poly cap is formed with an intersection of poly1 and poly2 that measures 10 x 20. (50 nm is the scale). what is the capacitance?

$$C = C_{ox}' \cdot A = 25\,fF/\mu m^2 \cdot (10 \times 0.05\,\mu m) \times (20 \times 0.05\,\mu m) =$$