① Quiz 3 on Wednesday.

a. # Diodes terminal characteristics

b. BJTs (npn)

② Midterm on Friday (55 min, close-book close-notes)

a. DAC

b. ADC

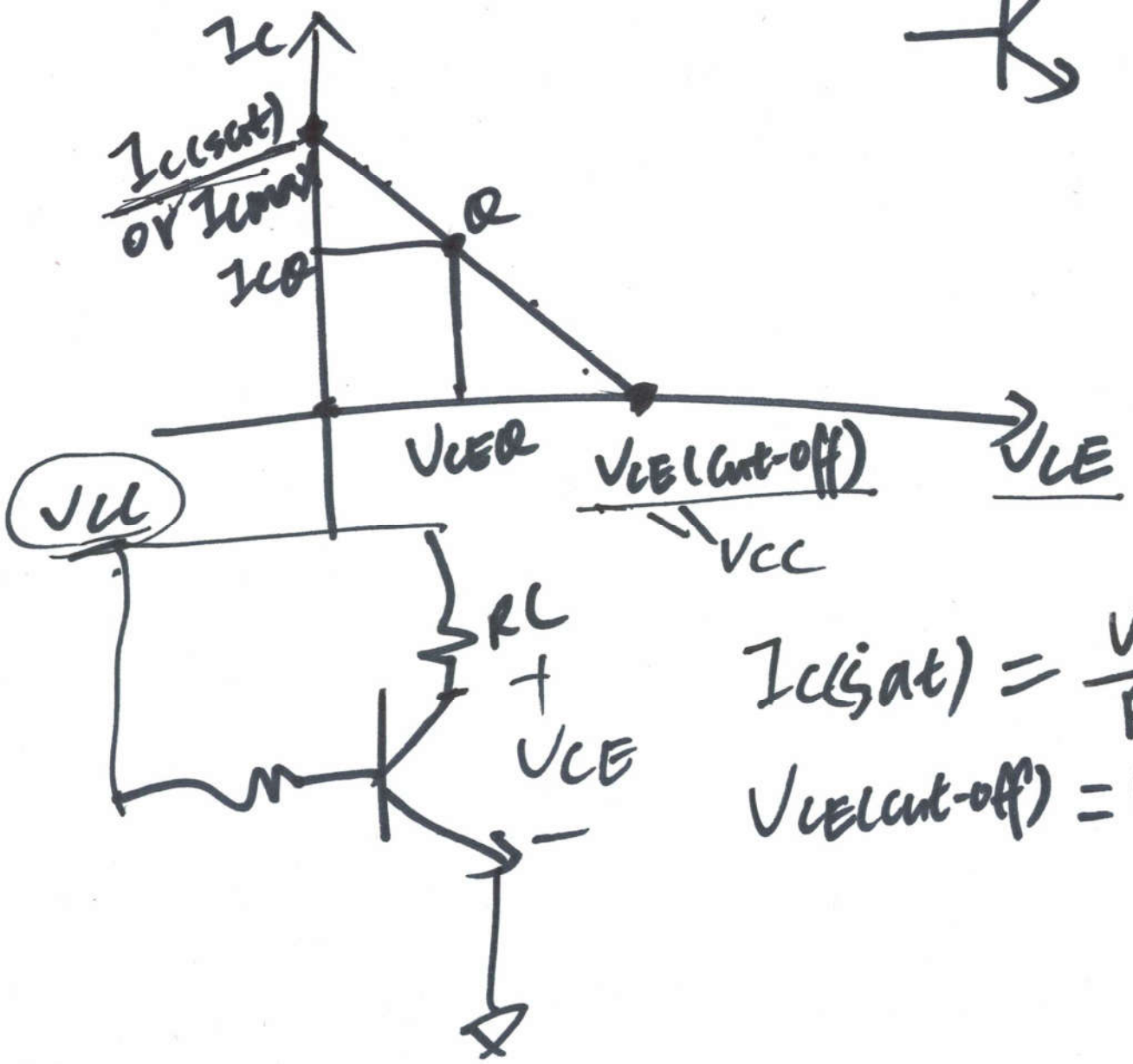
c. Diode terminal characteristics

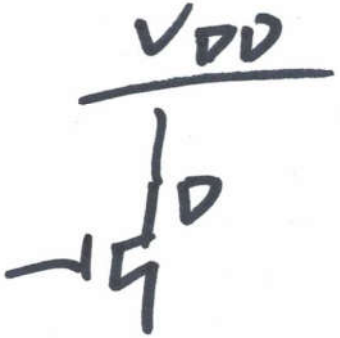
d. npns

e. concepts:

CLM, Latch-up, pn depletion region, Body Effect. I_S/I_D, N-well resistor sheet resistance. $n_i/n_n/n_p/P_n/P_p/N_A/N_D$.

load line



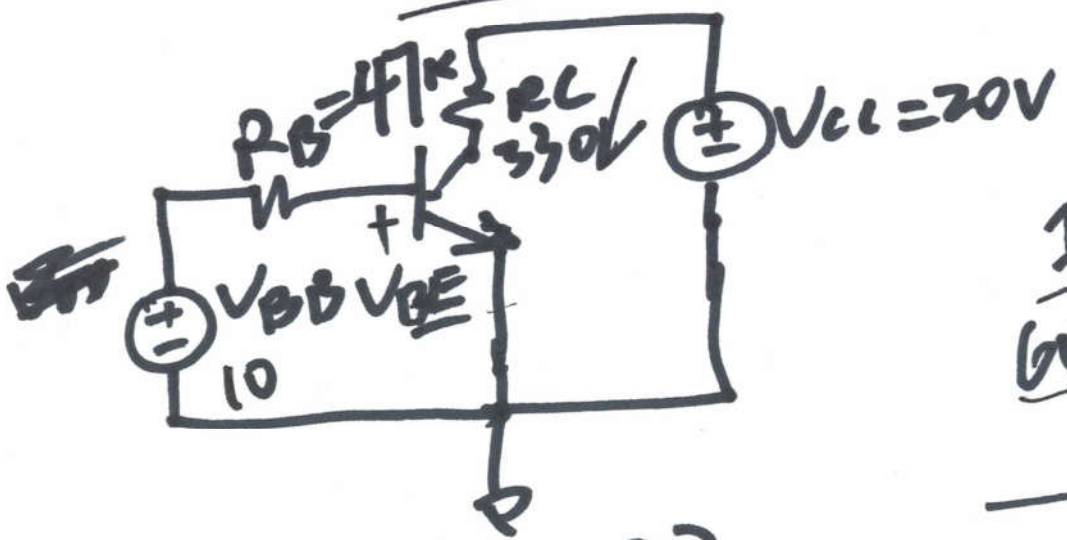


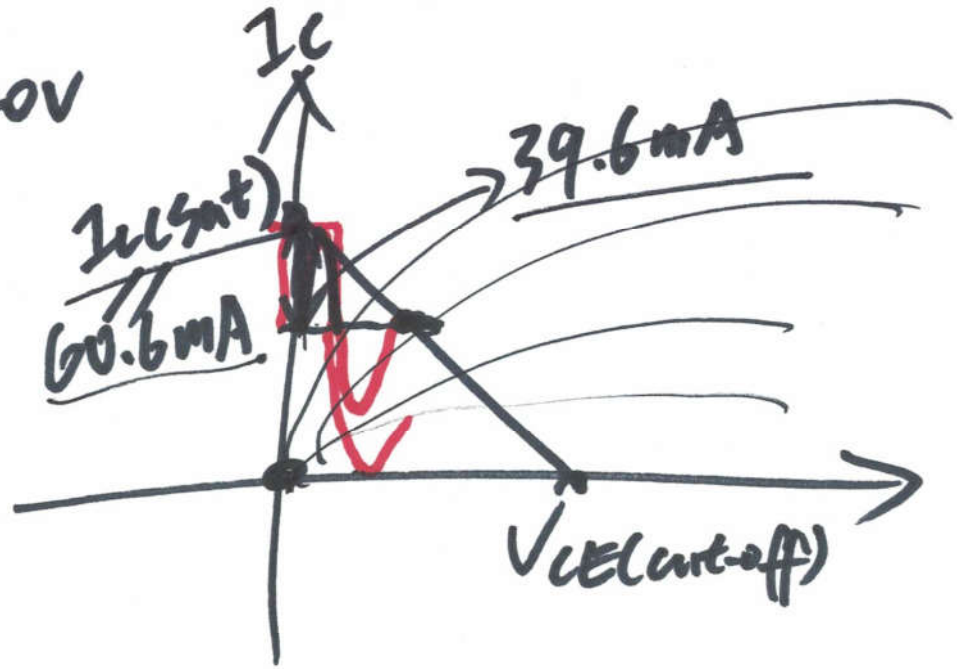
$$I_{C(sat)} = \frac{V_{CC}}{R_L}$$

$$V_{CE(cut\text{-}off)} = V_{CC}$$

Determine the Q-point and find the maximum peak value of the base current for linear operation.

Assume $\beta = 200$.





$$I_B = \frac{V_{BB} - 0.7}{R_B}$$

$$I_{CQ} = \beta \cdot I_B = 39.6\text{mA}$$

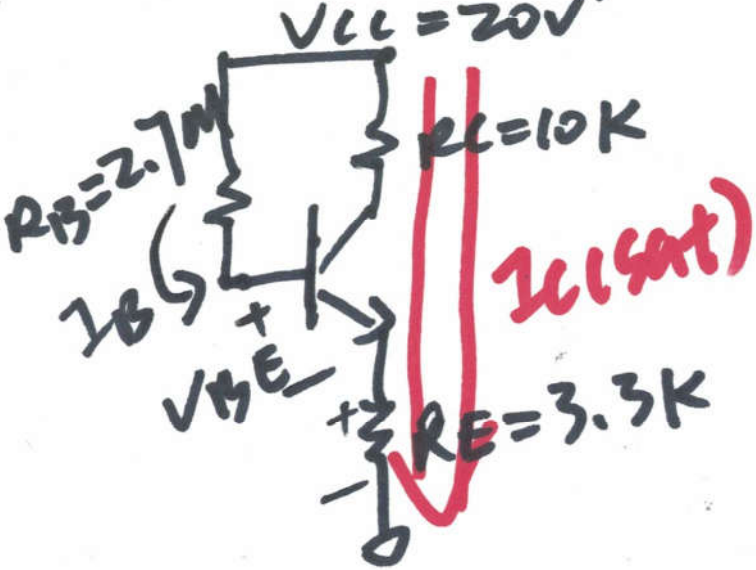
$$I_{C(sat)} = \frac{V_{CC} - 0}{R_C} = \frac{20V}{330} = 60.6\text{mA}$$

$I_{C(sat)} - I_{CQ}$
$= 60.6\text{mA} - 39.6\text{mA}$
$= 21\text{mA}$
which is the maximum swing for I_C.

Therefore, the peak value of the base current for linear operation is $\frac{21mA}{200} = I_{B(peak)}$ @

$= 105\,\mu A$

Example: Determine the @ point values of I_C, V_{CE}. Find $I_{C(sat)}$, $V_{CE(cut-off)}$, and construct the DC load line and plot the @ point. $\beta = 100$. (Assume $I_C = I_E$ to find $I_{C(sat)}$)



$$I_B = \frac{V_{CC} - V_{BE} - V_{RE}}{R_B}$$

$$= \frac{20 - 0.7 - V_{RE}}{2.7M}$$

$$= \frac{20 - 0.7 - (I_E \cdot R_E)}{2.7M}$$

$$= \frac{20 - 0.7 - ((1+\beta) I_B \cdot R_E)}{2.7M}$$

$\Rightarrow I_B = 6.37\,\mu A.$

$I_C = \beta \cdot I_B = 100 \cdot 6.37\,\mu A = 637\,\mu A = I_{CQ}$

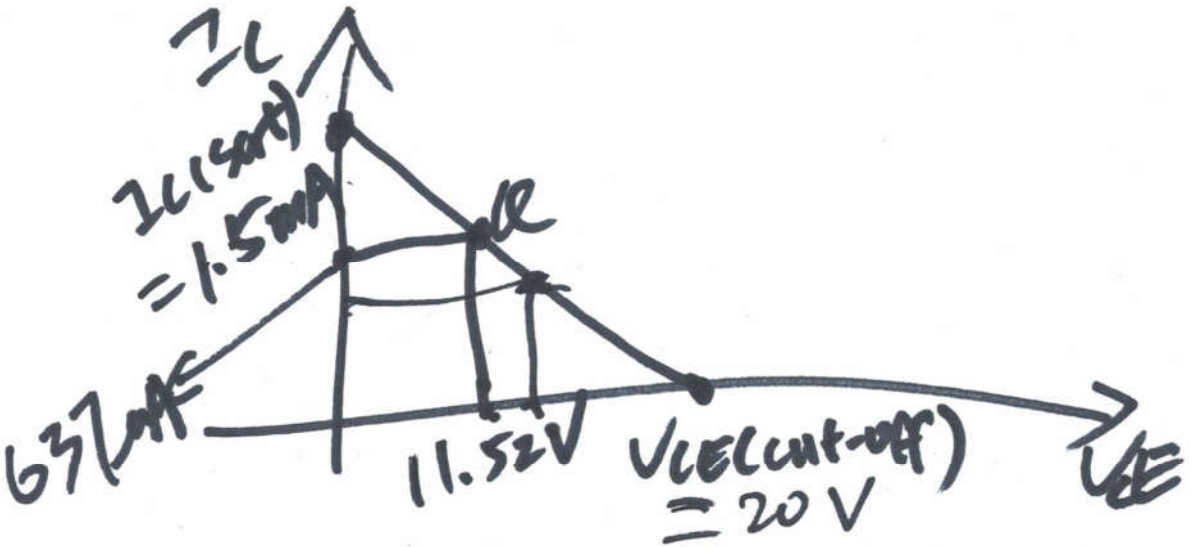
$I_E = (1+\beta) I_B = 101 \cdot 6.37\,\mu A = 643.37\,\mu A$

$V_{CE} = V_{CC} - I_C \cdot R_C - I_E \cdot R_E = 11.52V = V_{CEQ}$

when $V_{CE} = 0V$.

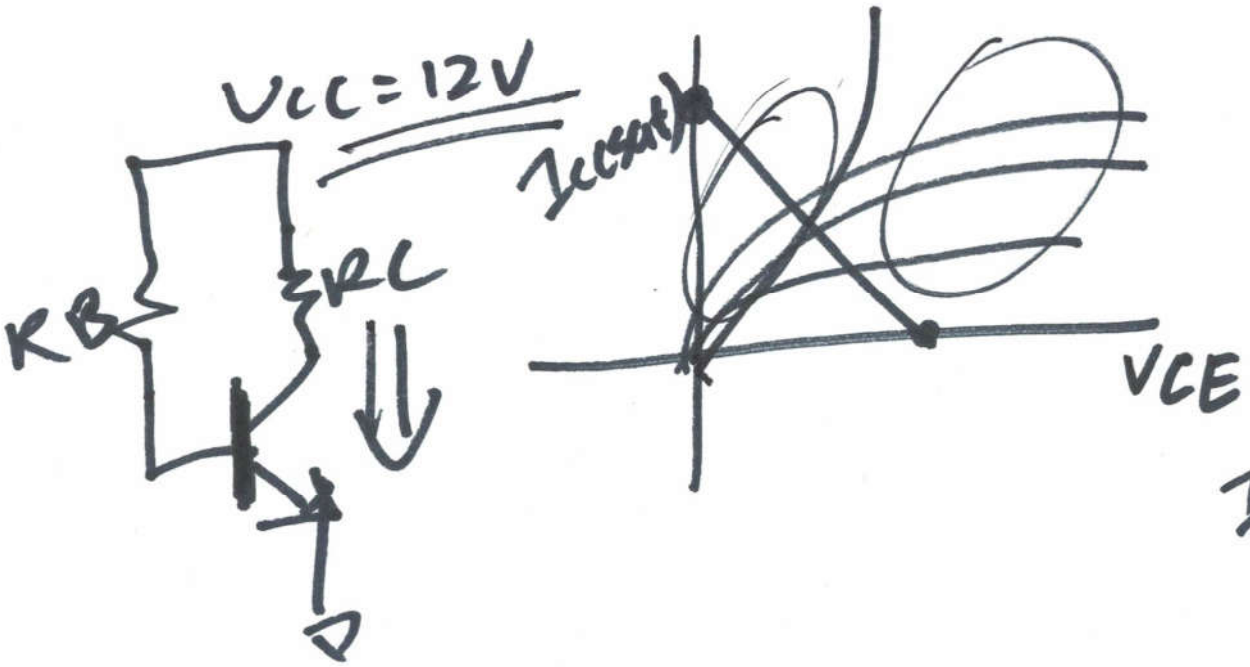
$I_{C(sat)} = I_{cmax} = \frac{V_{CC} - 0}{R_C + R_E} = \frac{20V}{10K + 3.3K} = 1.5\,mA$

$V_{CE(cut-off)} = V_{CC} = 20V$.



Example: Determine whether the transistor is biased in cut-off, saturation, or linear region. $\beta = 100$.

(a) $R_B = 75k$, $R_C = 1K$



$$I_{C(sat)} = \frac{V_{CC} - 0}{R_C} = \frac{12V}{1K} = 12mA.$$

$$I_B = \frac{12V - 0.7V}{R_B} = \frac{11.3V}{75K} = 0.15mA$$

$I_C = \beta \cdot I_B = 15mA > I_{C(sat)}$

so, it operates in the saturation region.

(b)

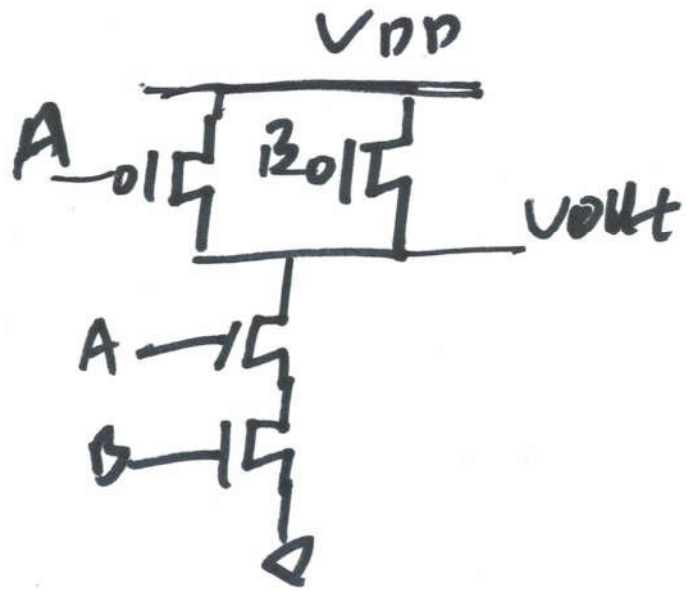
Static Logic Gates

Pmoses pull out to the power supply

Nmoses — — — — GND

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Stick Diagrams