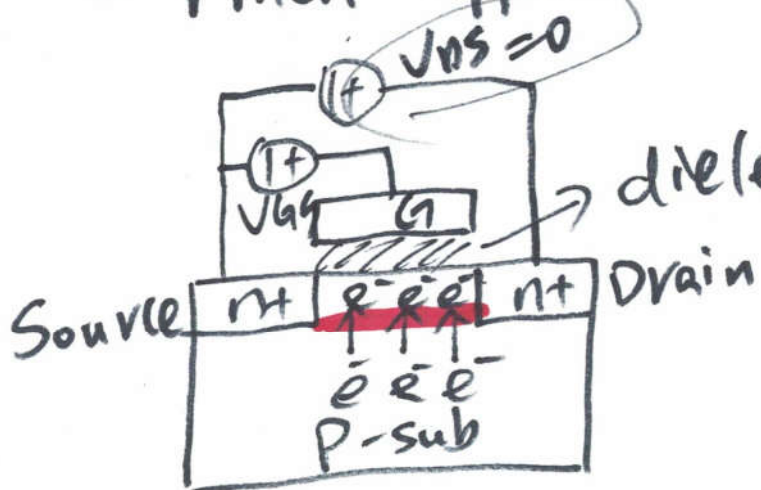
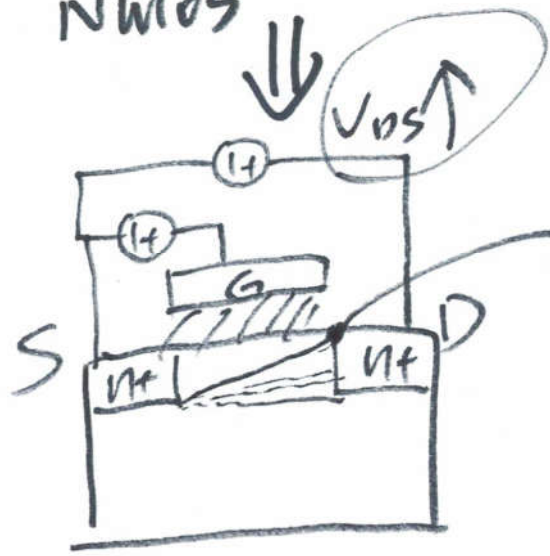


NMOS operation

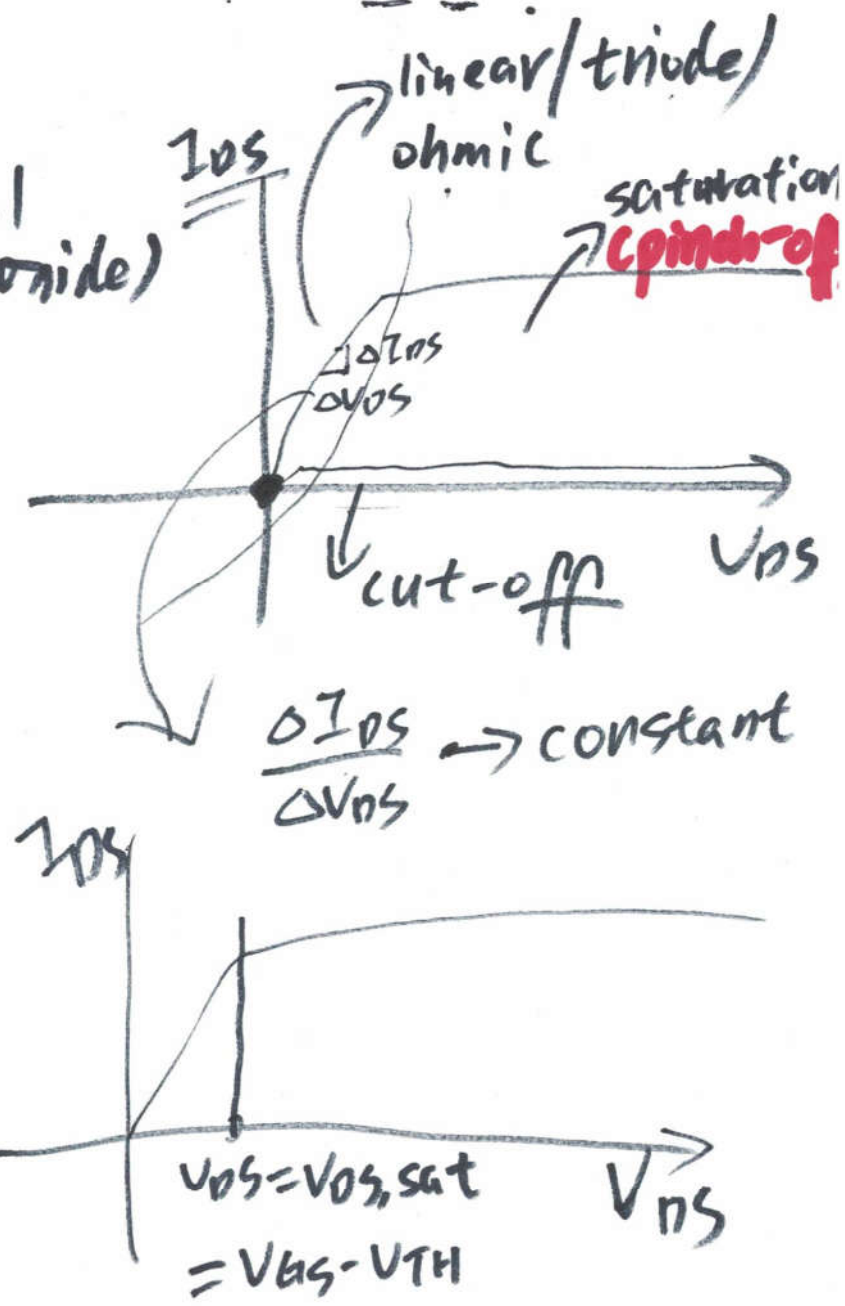
① Pinch-off

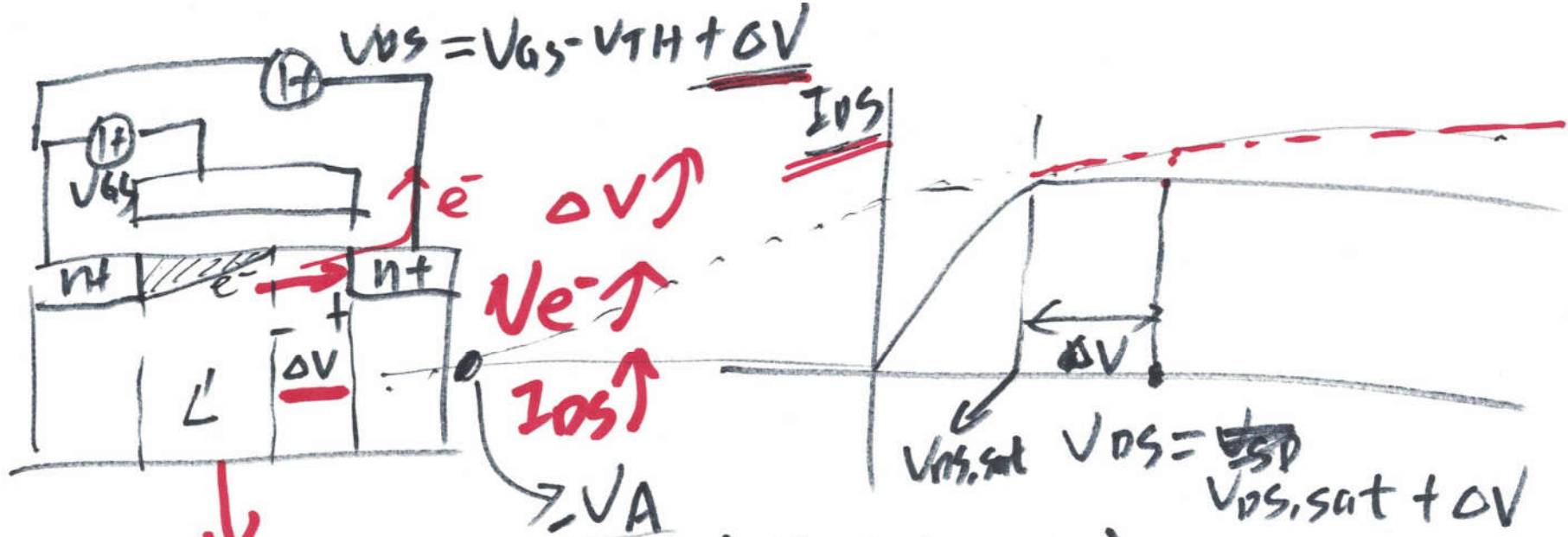


$V_{gs} > V_{TH}$ to turn on the NMOS



MOSFET

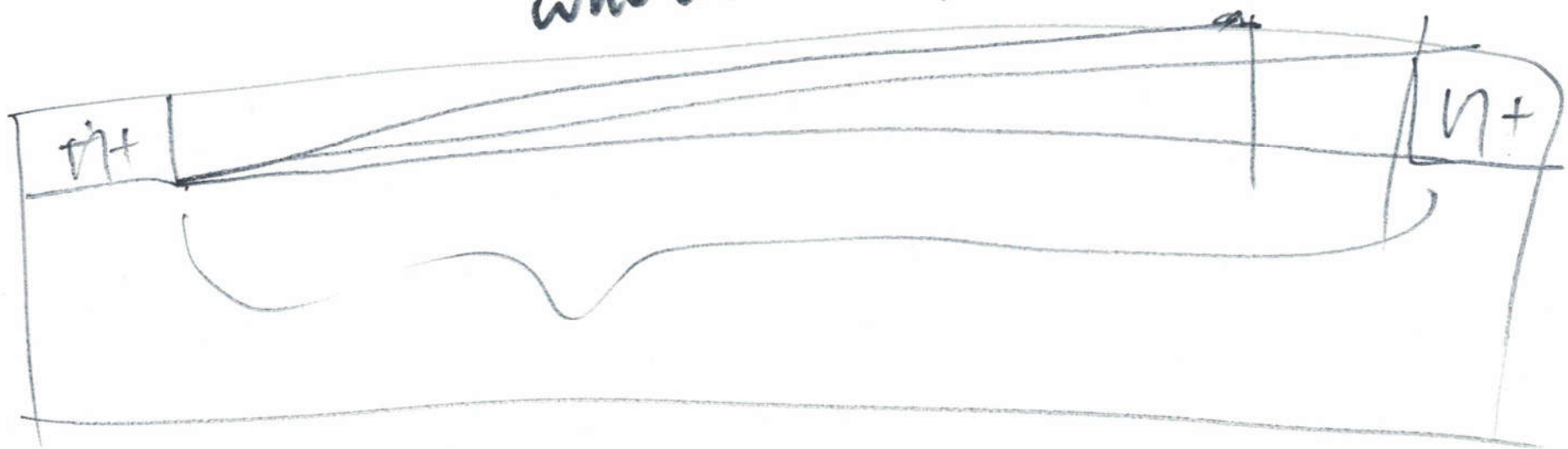




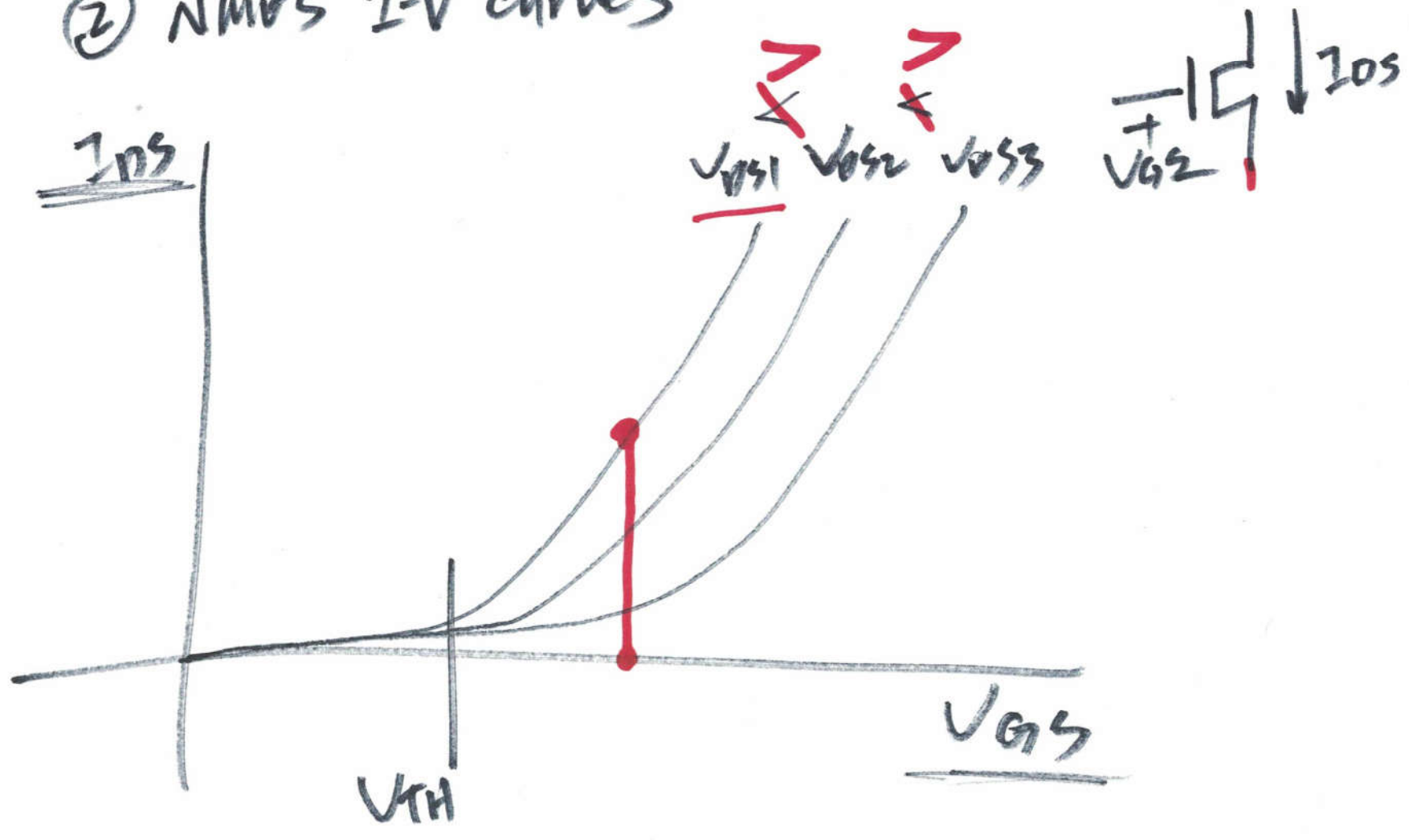
Channel Length Modulation (CLM)

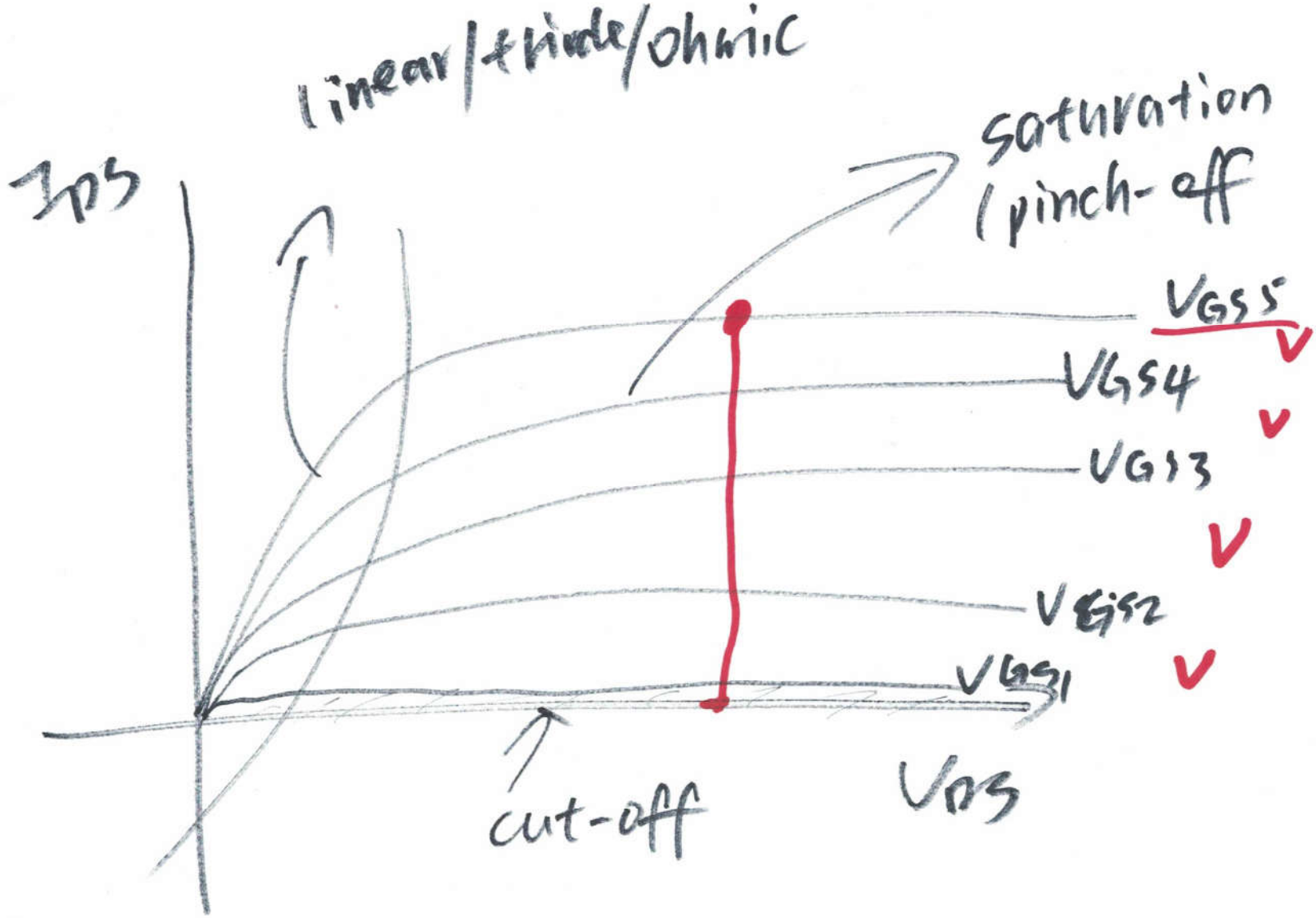
(~~aka~~ Early Effect)

→ (last name of the person who discovered this effect)



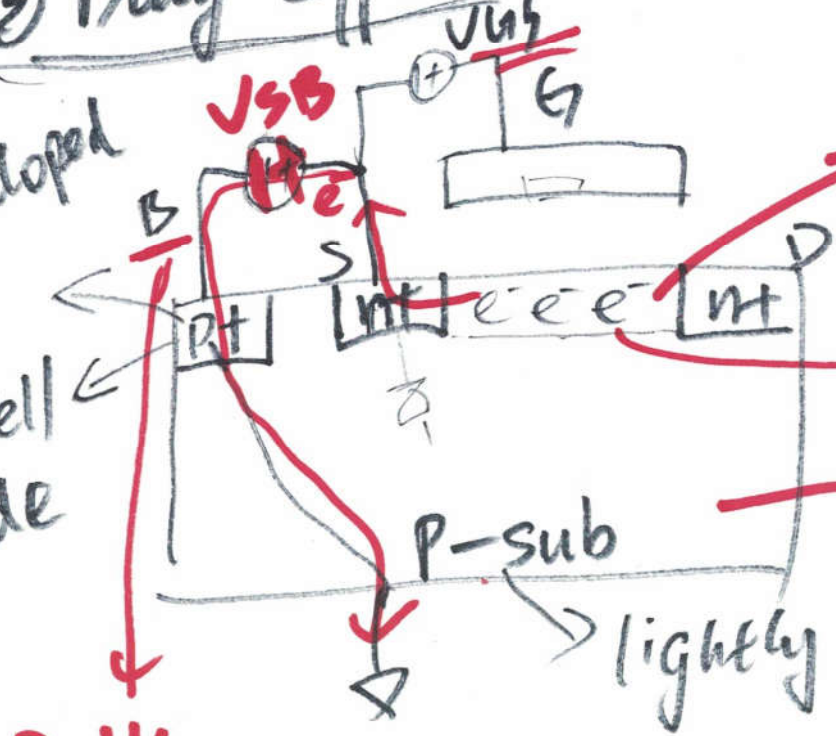
② NMOS I-V curves





② Body Effect

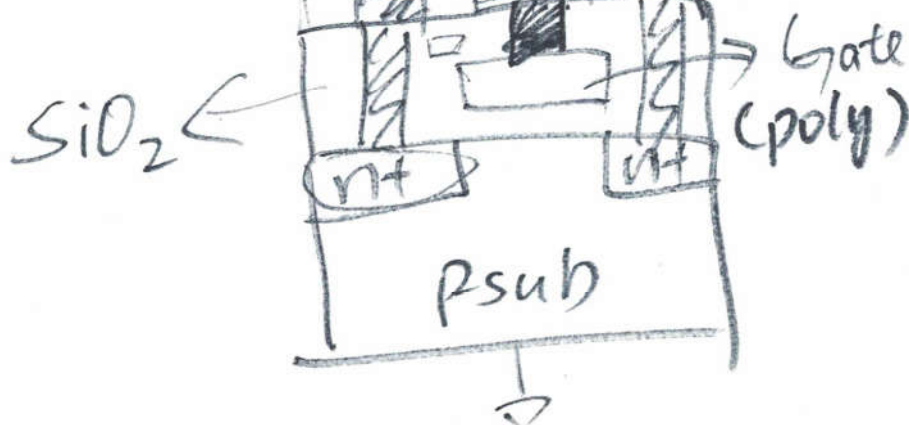
heavily doped
P-type
P-well
node

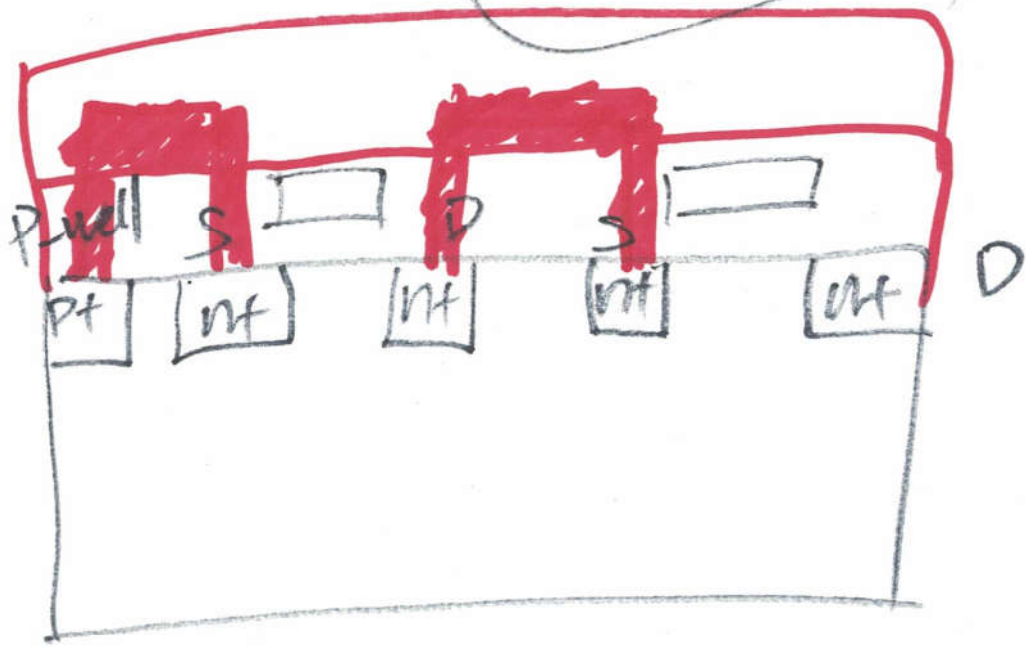
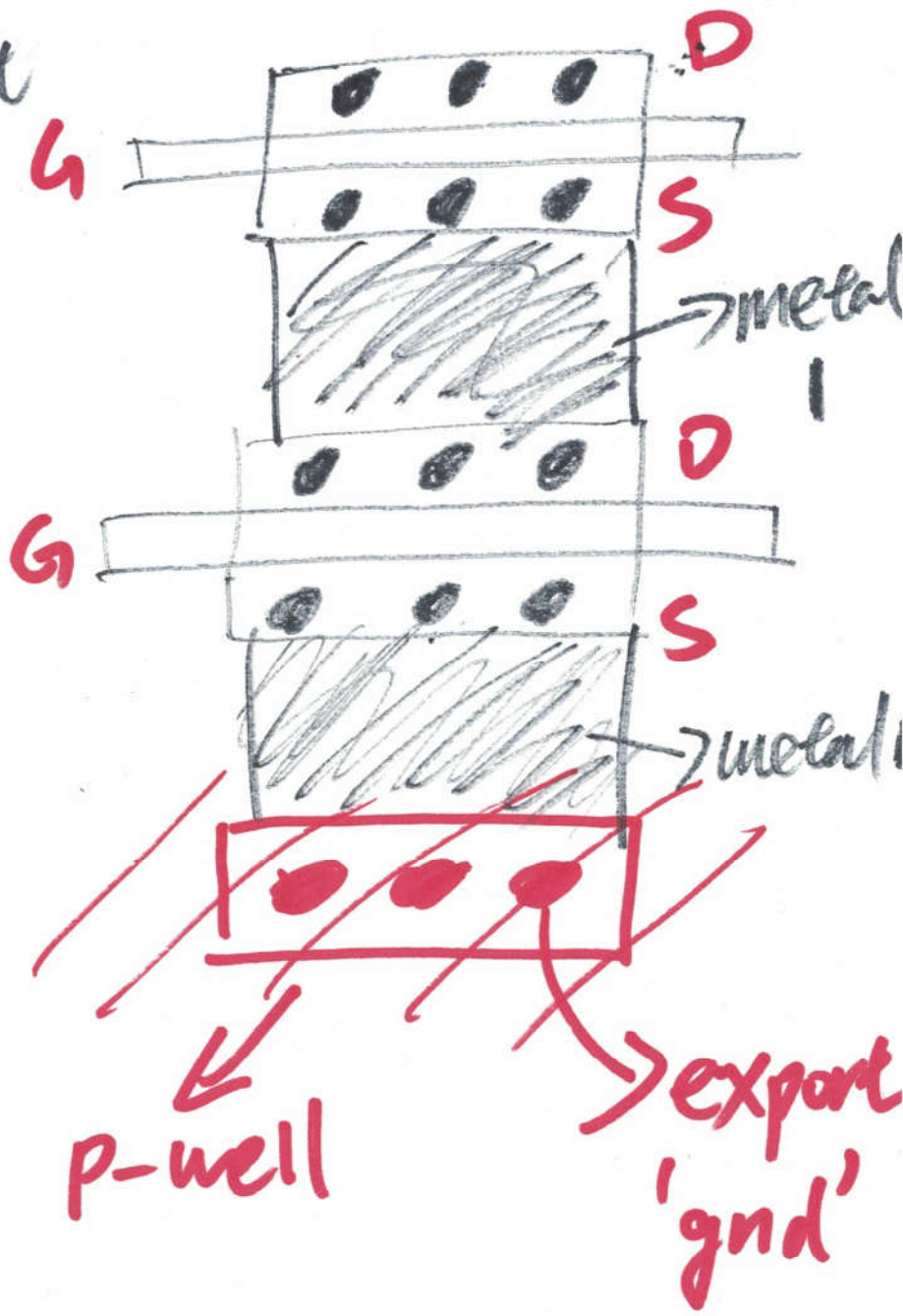
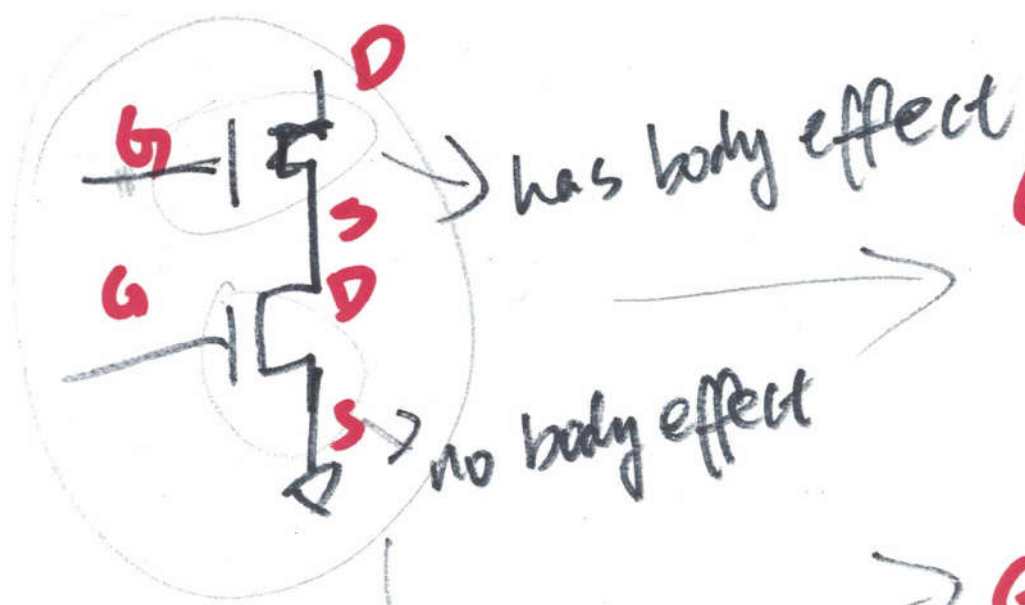


the channel is being inverted by V_{GS}
inversion layer

Bulk (Body)

or strong V_{GS} is needed





(6)

④ Latch-up

①

$P-N-P-N$
 $(b) \rightarrow K \rightarrow n(e) \rightarrow K \rightarrow P$
 \downarrow
 \downarrow

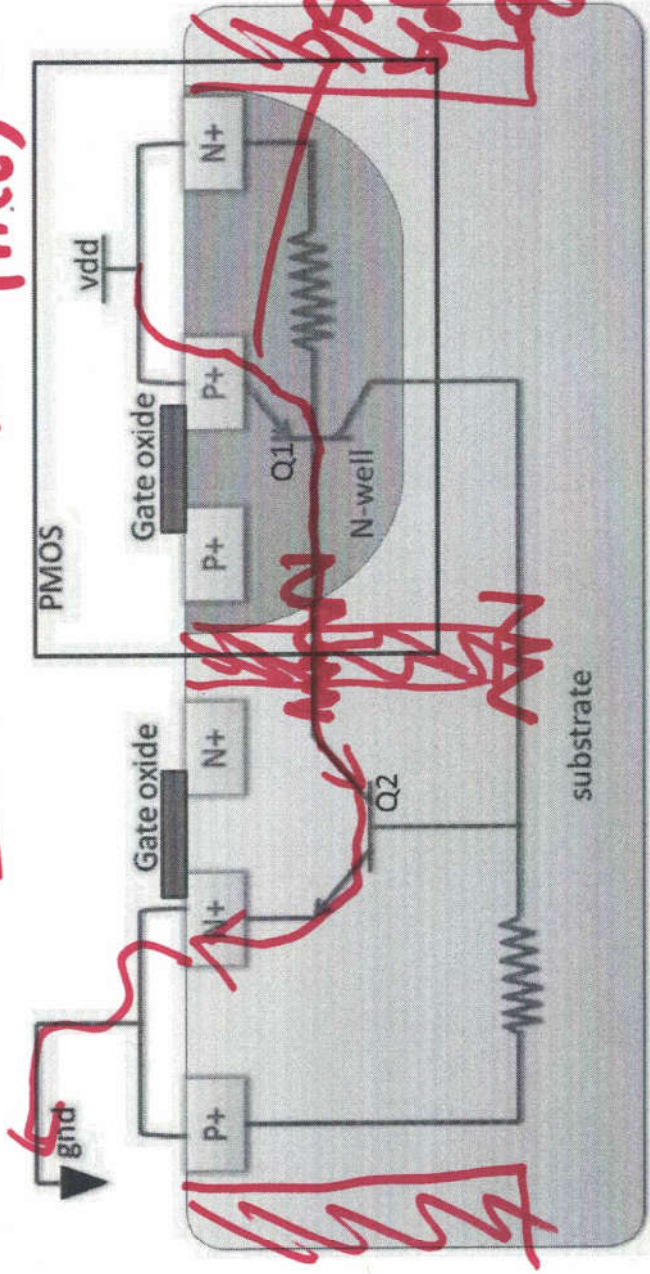
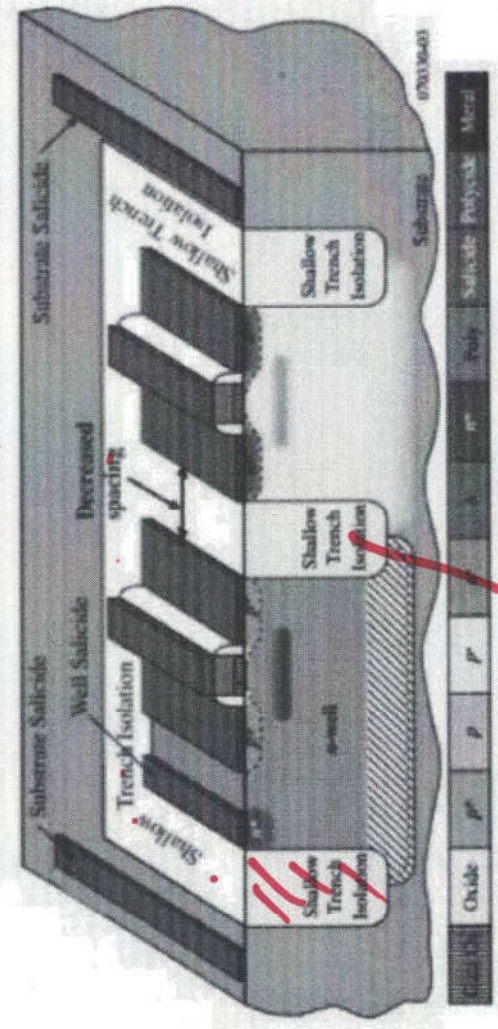


Figure 1 : Latchup formation in a CMOS device

USE OF SHALLOW TRENCH ISOLATION (STI) TECHNOLOGY

\hookrightarrow box isolation

- Use of Shallow Trench Isolation Technology: Shallow trench isolation (STI) allows closer spacing of transistors by eliminating the depletion region at the surface.



dielectric material
 made from SiO_2 , high ϵ_{ox} , low ϵ_{sub}