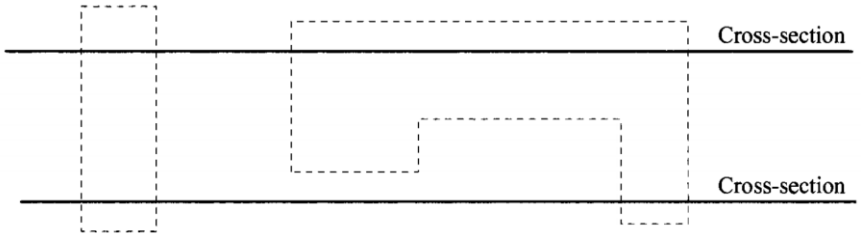
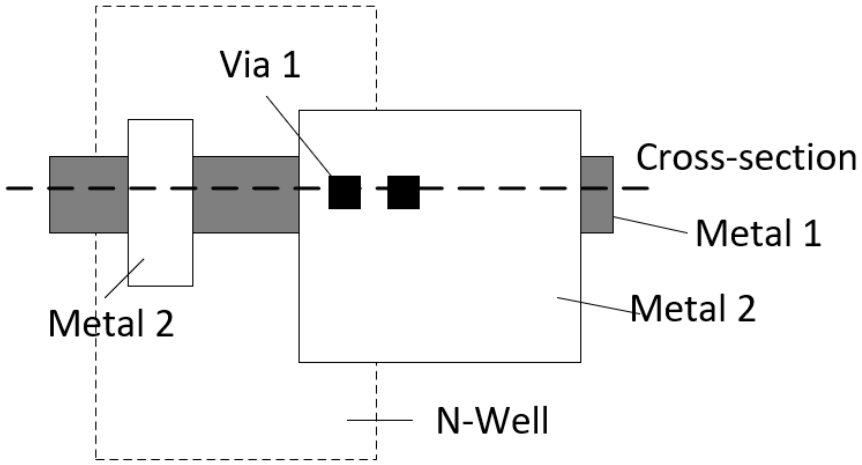
Chapter 4 CMOS Physical Layout (100 points)

1. For the layout of n-wells seen in the following figure (top view), sketch the cross-sectional views at the places indicated. Is there a parasitic pn junction in the layout? If so, where? (8 points)

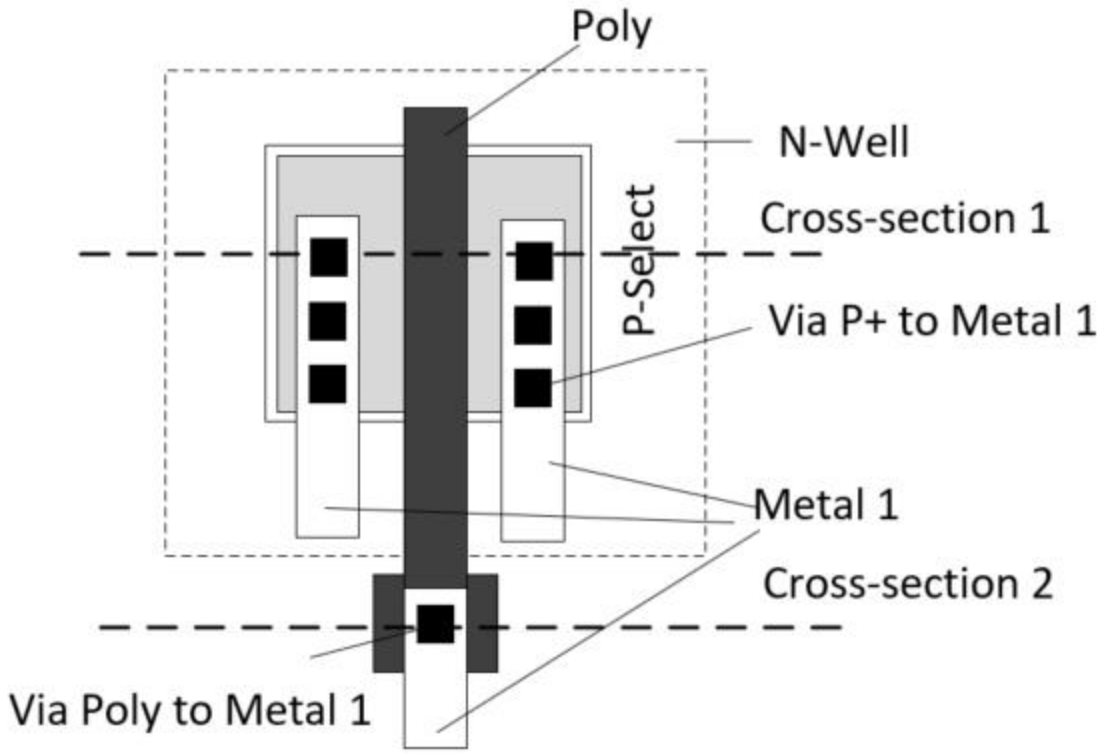


2. An n-well resistor has a width of 20 and a length of 400. A 20 by 20 square of n-well has a 15 fF parasitic capacitance. If the square resistance is 800 ohm, what is the time delay through this resistor without any extra load? (8 points)

3. The following figure shows the top-view of a layout. Draw the cross-sectional view of the location indicated by the dashed line. (8 points)



4. The following figure shows the top-view of a layout. Draw the cross-sectional views (cross-section 1 and cross-section 2 of the locations indicated by the dashed lines. (8 points)



5. Why is polysilicon's parasitic capacitance larger than Metal 1's? (8 points)

6. Draw the cross-sectional view of all the layers of the C5 technology (from P-sub to over-glass opening). (8 points)

7. Why the footprint of N-Select is larger than N-Active? (8 points)

8. In the CMOS fab process, how the gate (poly) is aligned directly on the top of the channel? (the channel length can be <10 nm). (8 points)

9. Can a polysilicon wire be used as resistors? (8 points)

10. How to reduce the resistance of a polysilicon wire? (8 points)

11. A poly-poly capacitor, the overlapping area of the two poly layers is 30 λ by 40 λ, Cox' is 25 fF/um^2 (λ is 300 nm). What is the capacitance of this capacitor? Draw the schematic and the layout of this capacitor in ElectricVLSI and run DRC/NCC checks (read the short tutorial in this link for how to draw a capacitor in ElectricVLSI). (20 points)