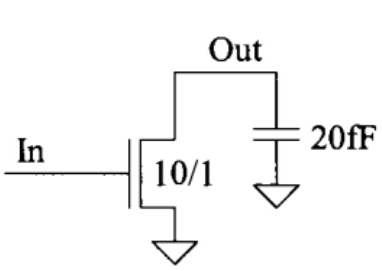
Chapter 5 Models for Digital Design (100 points)

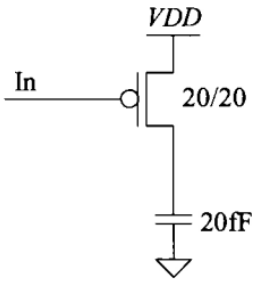
1. For the following circuits estimate the delay between the input and the output. Use the 50 nm (short-channel CMOS) process. (Table 10.2 is from the CMOS text book on page 320). (20 points)

Table 10.2 Parameters for general digital design using the long-channel (scale factor is 1 μm) or short-channel (scale factor of 50 nm) CMOS process **used in this book**.

Technology	Drawn	Actual size	$R_{n,p}$	$C_{ox,n,p}$
NMOS (long-channel)	10/1	10 μm by 1 μm	1.5k	17.5 *fF*
PMOS (long-channel)	30/1	30 μm by 1 μm	1.5k	52.5 *fF*
NMOS (short-channel)	10/1	0.5 μm by 50 nm	3.4k	625 *aF*
PMOS (short-channel)	20/1	1 μm by 50 nm	3.4k	1.25 *fF*



(a)



(b)

2. Regenerate Figure 11.14 in the CMOS book (P341) using the 50nm technology in LTSpice. Then build the same circuit using the 1um technology (PMOS: 30um/1um, NMOS: 10um/1um, Table 10.2). Calculate the oscillation frequency and compare the result with the simulation. (20 points)

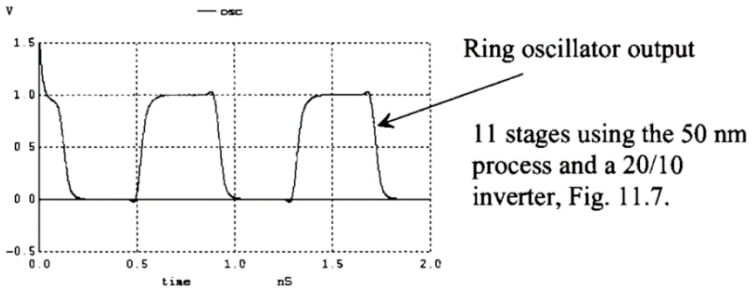
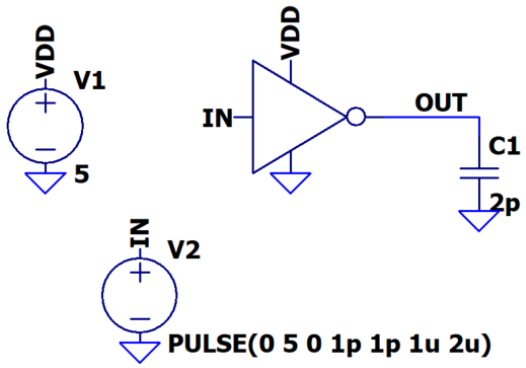


Figure 11.14 Oscillation frequency for the ring oscillator described in Ex. 11.7.

3. Draw the resistive/capacitive digital model and estimate the oscillation frequency of a 7 stage ring oscillator. NMOS: Rn = 3.4 k, Coxn = 0.625 fF. PMOS: Rp = 3.4 k, Coxp = 1.25 fF. (20 points)

4. What is the dynamic power dissipation of the following circuit? (Assume the inverter has adequate current to drive the load capacitor, also Cload = Ctot) (20 points)



5. Build a TG based DFF (edge triggered) in ElectricVLSI. Run the simulation to verify the logic. Layout the circuits using ElectricVLSI, run DRC and NCC checks. (Refer to Figure 13.22 on Page 387 of the CMOS book). (20 points)

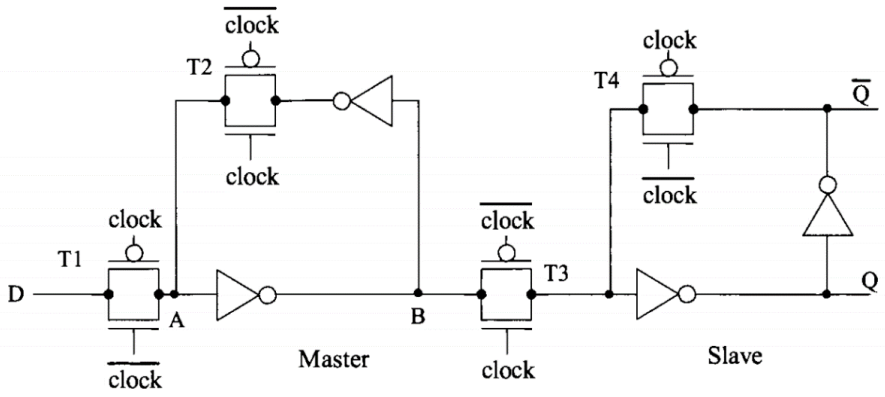


Figure 13.22 An edge-triggered D-FF.