

HW 5 AOI Logic Circuits Simulation

1. Implement XOR and XNOR gates using AOI logic in ElectricVLSI. Verify the logic using simulations. Use the C5 model file. (no layout is needed). (25 points)
2. Use ElectricVLSI to design a 3-bit subtractor (2's complement). Use XOR gates as the control units. Use the C5 model file. Verify the logic by simulating at least three input combinations. (schematic only, no layout). (25 points)
3. Use ElectricVLSI to design a 3-bit subtractor (2's complement). Use MUXes as the control units. Use the C5 model file. Verify the logic by simulating at least three input combinations. (schematic only, no layout). (25 points)
4. Verify AOI logic for a 1-bit Full Adder (Page 367 of the textbook) by hand using logic equations/theorems. Build it in Electric VLSI and verify the logic using simulations (use the C5 model file, schematic only, no layout). (25 points)