ENGR337 Spring 2018 Homework

Chapter 1 Circuit Basics and LTSpice

1.1 Use KCL and KVL to solve the current/voltages in the following circuit.

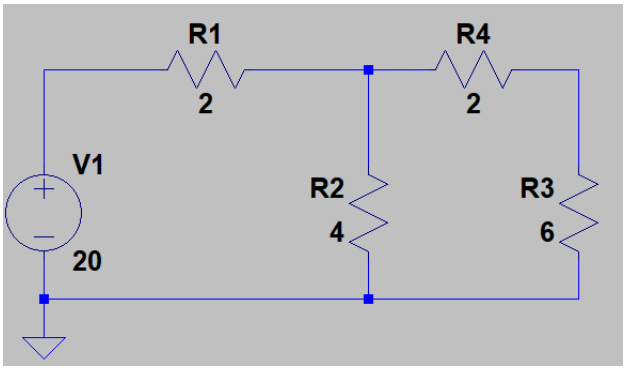
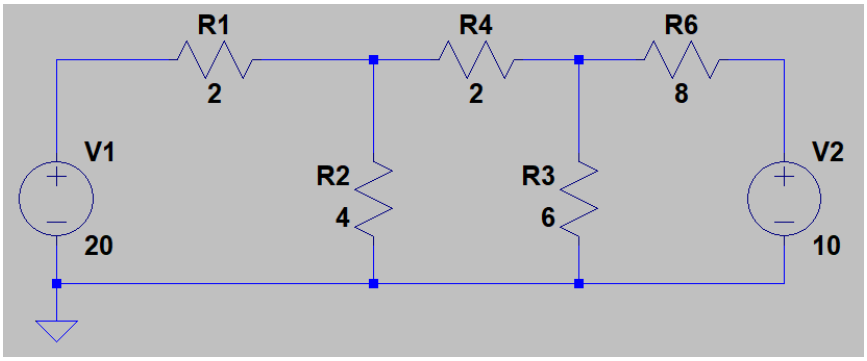


Fig. 1.1

1.2 Use the Mesh Current method to solve the current/voltages in the following circuit.

(a)



(b)

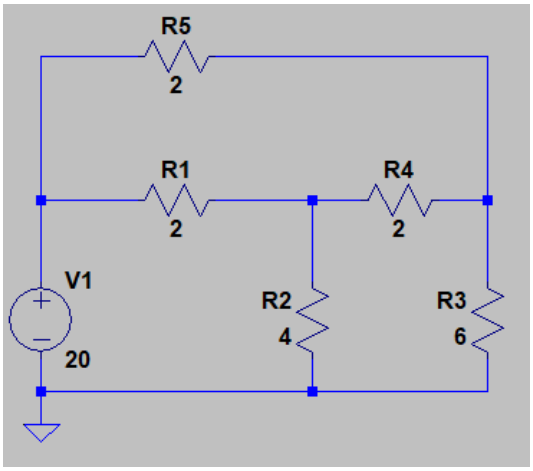


Fig. 1.2

1.3 Use the Super Mesh Current method to solve the current/voltages in the following circuit.

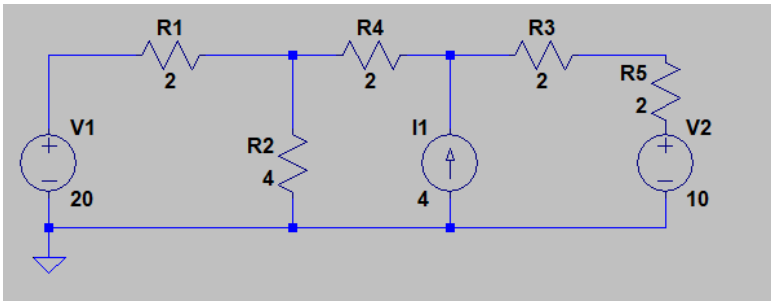


Fig. 1.3

1.4 **Convert** the following circuit into it's **Thevenin's equivalent circuit**, then **calculate** the current flows through the load resistor.

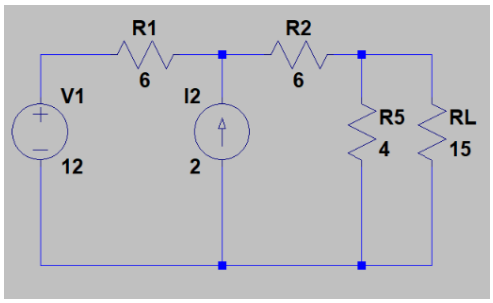


Fig. 1.4

1.5 **Convert** the following circuit into it's **Thevenin's equivalent circuit**, then **calculate** the current flows through the load resistor.

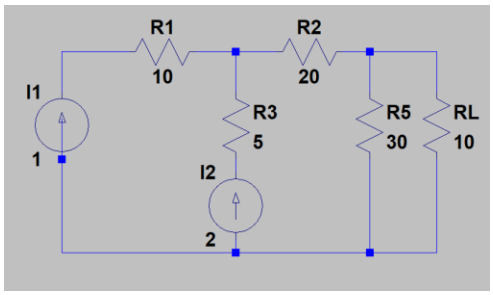


Fig. 1.5

1.6 **Convert** the following circuit into it's **Norton's equivalent circuit**, then **calculate** the current flows through the load resistor.

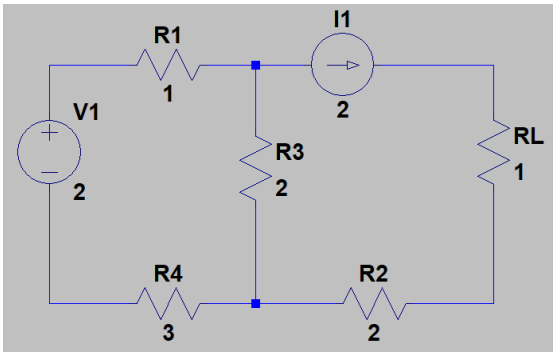


Fig. 1.6

1.7 **Convert** the following circuit into it's **Norton's equivalent circuit**, then **calculate** the current flows through the load resistor.

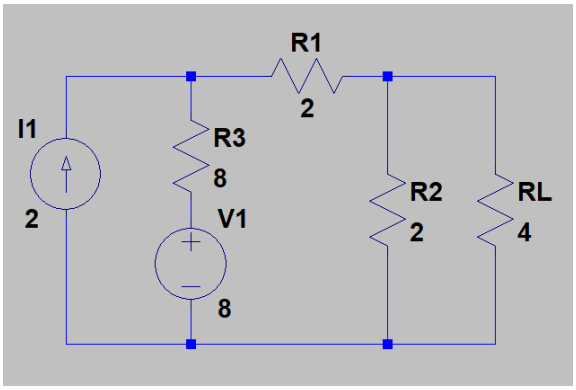


Fig. 1.7

1.8 Calculate |Vo/Vi|, and the time delay. Hand draw the input the output signal, and also show the time delay on the graph. Finally, compare the results to your simulation. V1: amplitude 1V (Vpp 2V), f=100 kHz.

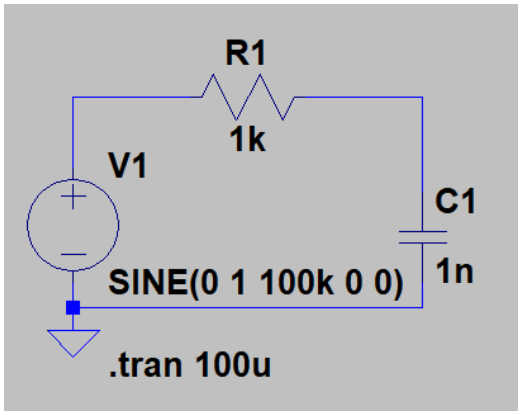
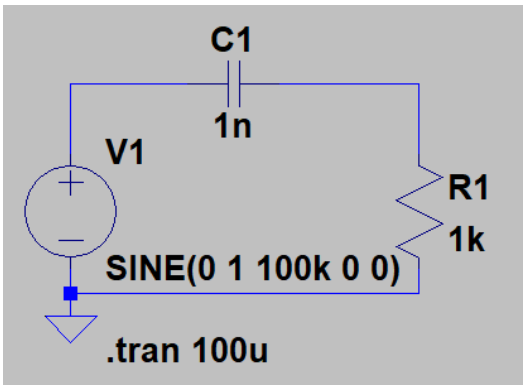


Fig. 1.8

1.9. Calculate |Vo/Vi|, and the time delay. Hand draw the input the output signal, and also show the time delay on the graph. Finally, compare the results to your simulation. V1: amplitude 1V (Vpp 2V), f=100 kHz.



1.10. Calculate |Vo/Vi|, and the time delay. Hand draw the input the output signal, and also show the time delay on the graph. Finally, compare the results to your simulation. V1: amplitude 1V, f=100 kHz.

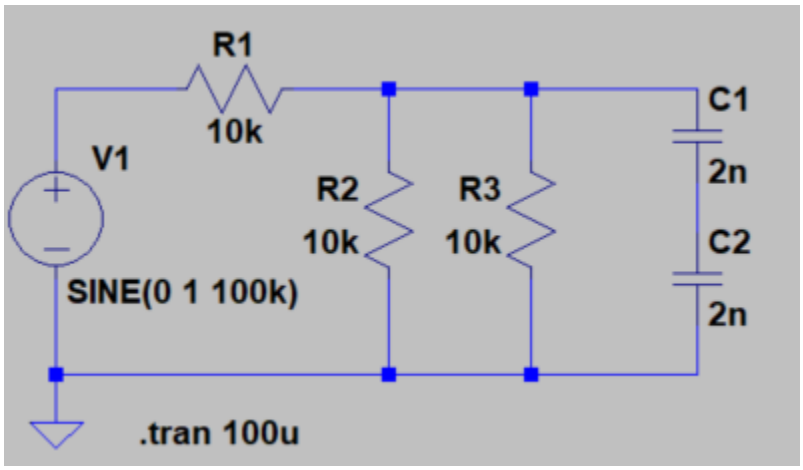


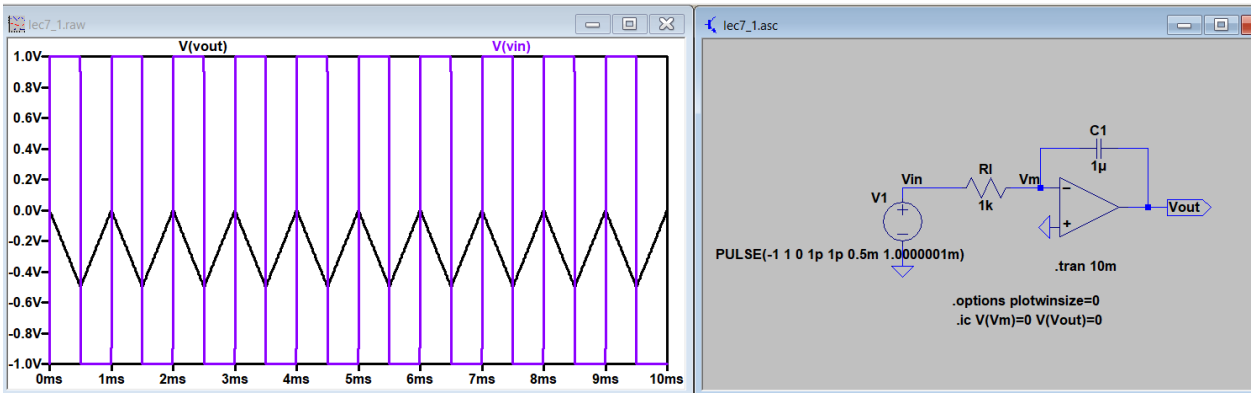
Fig. 1.10

Chapter 2 Operational Amplifiers (OpAmp)

2.1. 1) Use LTSpice, use the E1 voltage amplifier, create a symbol to make it in the standard OpAmp triangle shape like I showed in the lecture. 2) Use this OpAmp to build an inverting amplifier and a non-inverting amplifier. 3) Derive the voltage gain for these two amplifiers, and use LTSpice to verify the gain.

2.2. In the following integrator, Vo is charged to -0.5 V – 0 V. Modify the value of the resistor or the capacitor, to make the Vo swings between -1 V – 0V. (Do not change anything about the voltage source).

(Show the calculations and the simulations for credit).



2.3 Based on the following circuit, design the values of the capacitor and the resistor to make the cutoff frequency to be 5 kHz. Use LTSpice to verify the cutoff frequency.

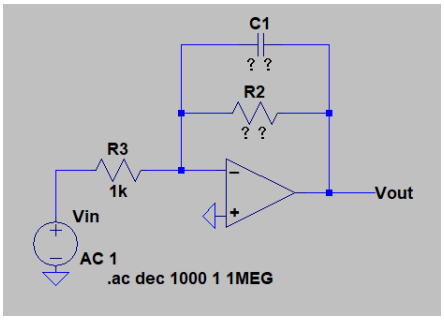


Fig. 2.3

2.4 Derive the voltage gain of both the inverting OpAmp and the non-inverting OpAmp when the open-loop gain of the OpAmp is not infinite (a finite gain of ***A***).

2.5 Derive the differential gain and the common mode gain of the following difference amplifier. Then, show the common-mode rejection ratio (CMRR). (Assume R2/R1 = R4/R3, or say, R2=R4, R1=R3).

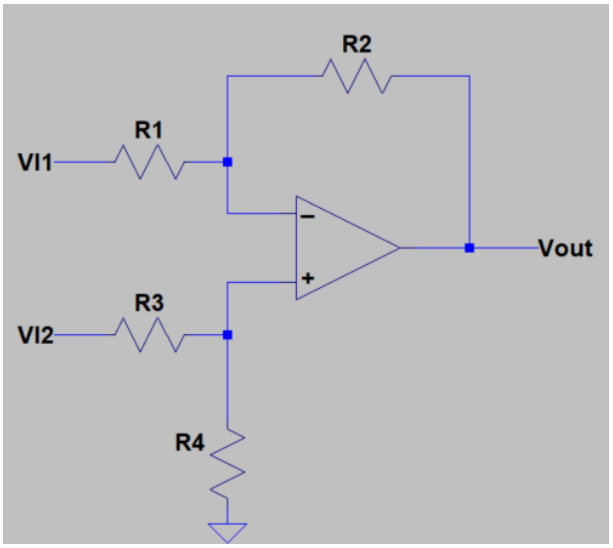


Fig. 2.5

2.6 Derive the voltage gain of the following instrumentation amplifier.

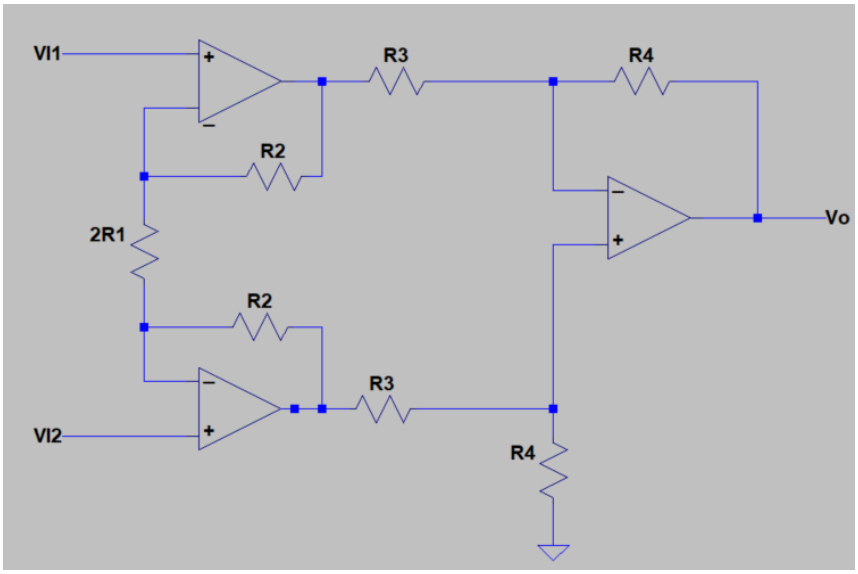


Fig. 2.6

Chapter 3 The pn Junction, and the diode

3.1 Draw the pn junction and explain:

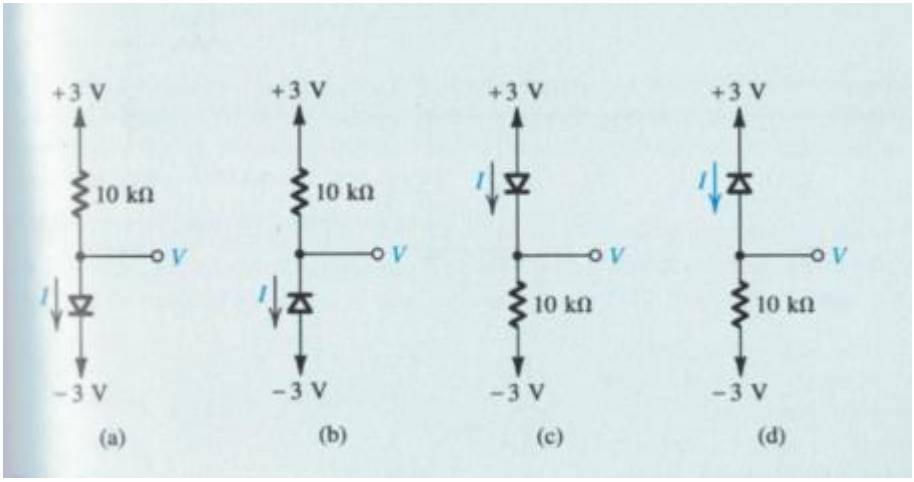
1) Without an external voltage, the formation of a depletion region, and the formation of the diffusion current and the drift current.

2) With an external voltage, explain the changes of the width of the depletion region under 'forward bias' and 'reverse bias' operations.

3) Explain how the depletion region will be changed, and how the diode capacitance will be changed with an increasing voltage under both 'forward bias' and 'reverse bias' operations?

3.2 Ideal diodes, find the values of the voltages and currents indicated in Fig. 3.2 (a-b)

(a)



(b)

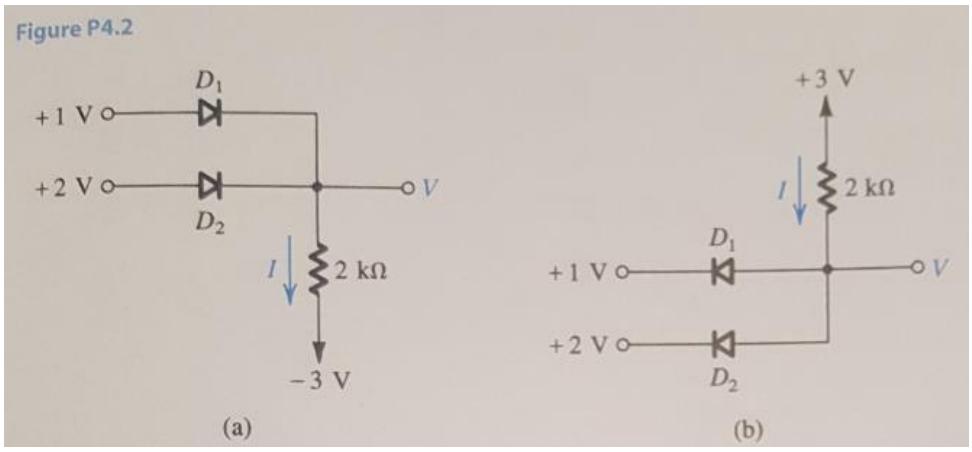


Fig. 3.2

3.3 In Fig. 3.3, Vi is a 1k Hz 5-V peak-peak sine wave (centered at 0V), sketch the waveform of Vo and label the peak values.

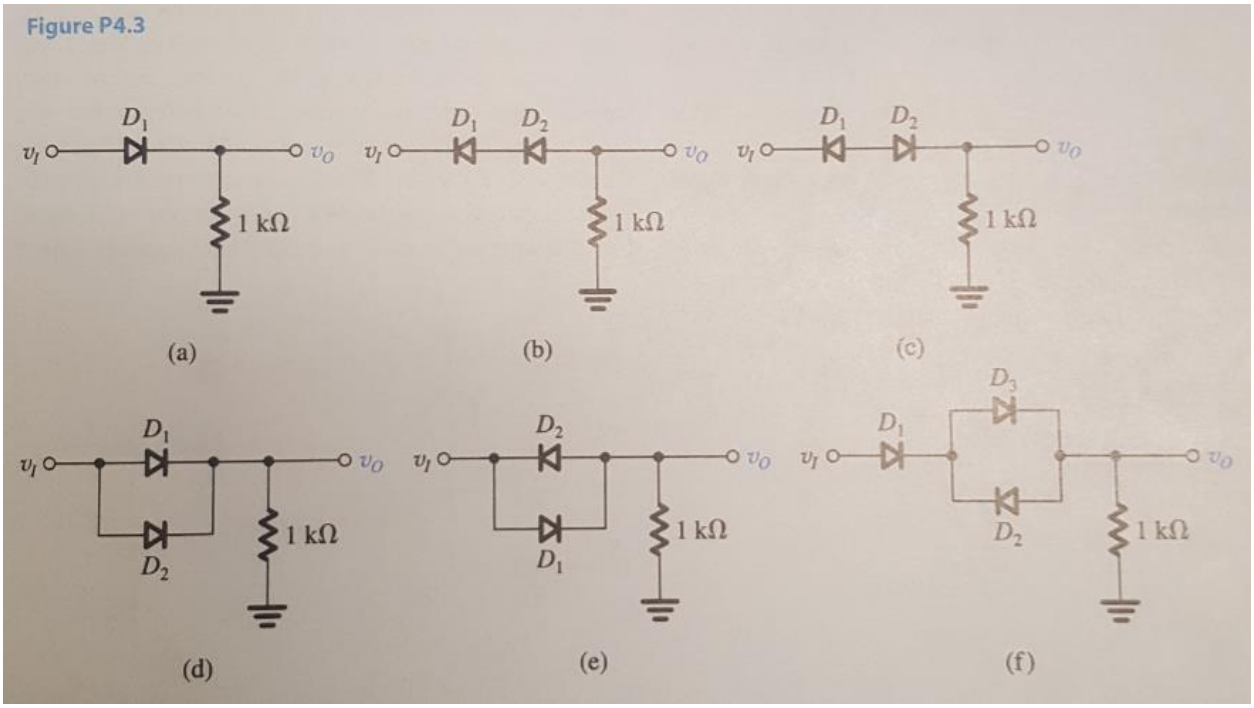


Fig. 3.3

3.4 Design a voltage multiplier (a high voltage DC power supply), the input voltage is a (-5V,5V) peak-peak square wave, the output should be at least 40 V DC. However, the working load is a 50 pF capacitor, the maximum voltage can be applied to the cap is 20 V. Use this HV power supply to drive this capacitor without burning it. (you may need a Zener diode to protect your circuit). (Use LTSpice to design the circuit and demonstrate your design).

Chapter 4 The MOSFETs

**KP and Vth can be found in model.txt

4.1. (1) Build the circuit using nmos in LTSpice, and change the VGS values to 'list 1.5 1.8 2', and simulate the 'VDS vs ID' curve. (2) Use a fixed VGS voltage and change the variable to VDS, and use '.step param VDS list 2 3 4 5', and simulate the 'VGS vs ID' curve. Show your simulation on a printed paper for credit.

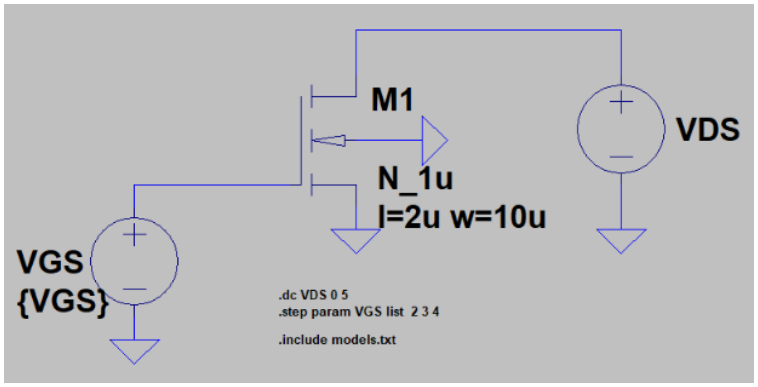
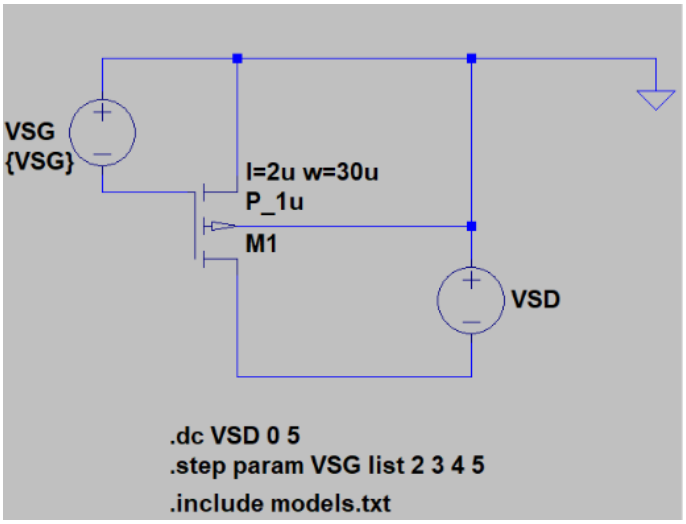


Fig. 4.1

4.2. Repeat the problem above for the PMOS circuit below: (please note that it is VSG/VSD now, and the PMOS substrate is connected to the highest potential in the circuit). Show your simulation on a printed paper for credit.



4.3. Draw a figure to explain the 'Body Effect'.

4.4. Calculate I_D of the NMOS and verify with LTSpice. Show your calculation/simulation on a printed paper for credit.

**KP and Vth can be found in model.txt. Use the N_1u model for this problem.

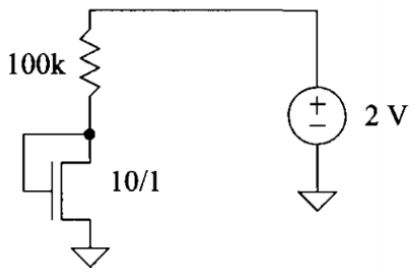


Fig. 4.4

4.5. Calculate I_D of the PMOS and verify with LTSpice. Show your calculation/simulation on a printed paper for credit.

**KP and Vth can be found in model.txt. Use the P_1u for this problem.

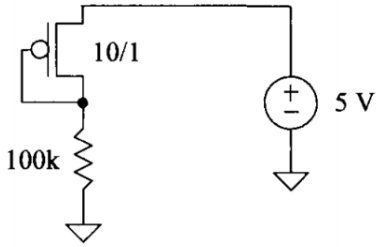


Fig. 4.5