CE433 Embedded Devices Spring 2022 midterm exam (100 points)
11:15 am – 12:40 pm, 3/15 Tuesday
Open book, open notes, open internet
Submit the results (PDF) to yli@fortlewis.edu by 12:40 pm on 3/15

1. Show the UQ16.16 fixed point representation of $25.25_{(10)}$. (3 points)

2. Show the floating-point representation of $25.25_{(10)}$ (half precision). (3 points)

3. Show the floating-point representation of $-25.25_{(10)}$ (half precision). (3 points)

4. Show the process of floating point addition of the following operation. (3 points)

(a) 21.125 + 6.5

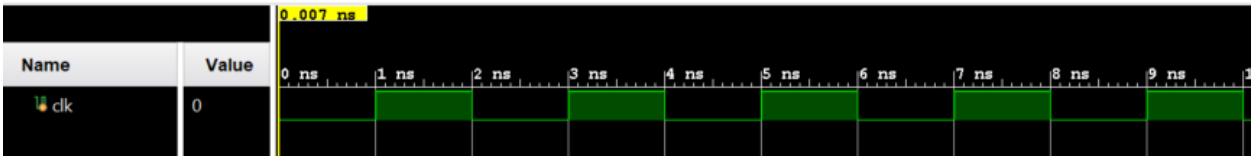
5. What are the total number of pixels horizontally and vertically in the VGA 640 x 480 @ 60 Hz industry standard timing? (3 points)

6. Which 'z' has the new x and y values if the following two blocks are being executed separately and only once? (5 points)

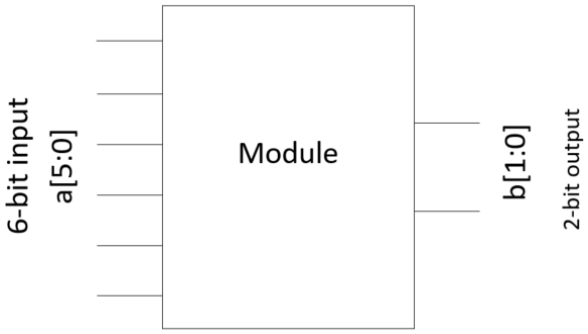
```
 1 always @(posedge clk)
 2 begin
 3         x=a|b;
 4         y=a&b;
 5         z=x|y;
 6 end
 7
 8 always @(posedge clk)
 9 begin
10         x<=a|b;
11         y<=a&b;
12         z<=x|y;
13 end
14
```

7. Write a Verilog module for the 3:1 multiplexer that uses the '?:' operator. A 3:1 multiplexer has 3 input lines, 2 select lines and an output line which is driven by one of input lines based on select inputs. (no simulation is required, just type it in Gvim). (5 points)

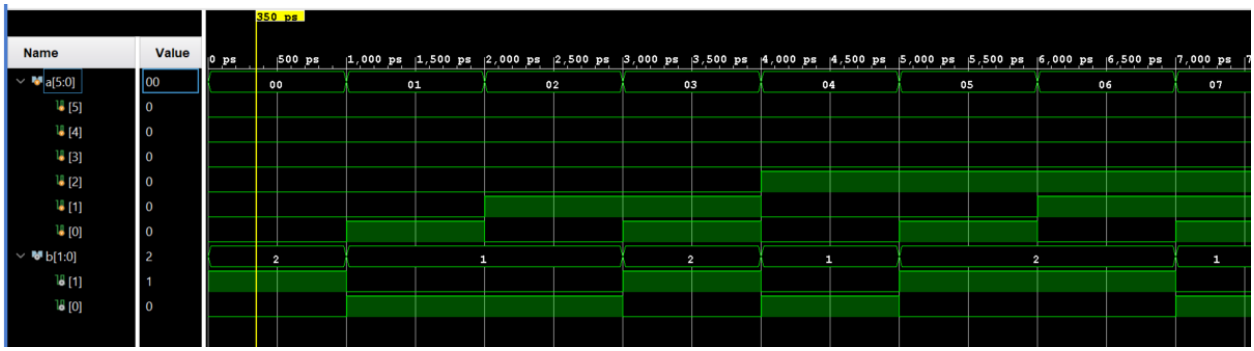
8. In Vivado simulation, make a 2 ns period clock waveform. Show the code and the simulation results for credits. (15 points)



9. Design a module which has a 6-bit input bus. The module checks if there are even number of one's or odd number of one's in the input. The two output bits shows output =10 when it's even, shows output = 01 when it's odd. Show simulation results that displays both outputs. (30 points)



A similar simulation result as follows:



10. Refer to the Sequential Circuit tutorial, Section 3. Use the behavioral form to create a module for the following state diagram. Design the testbench to verify the logic. Show simulation results for credits. (30 points)